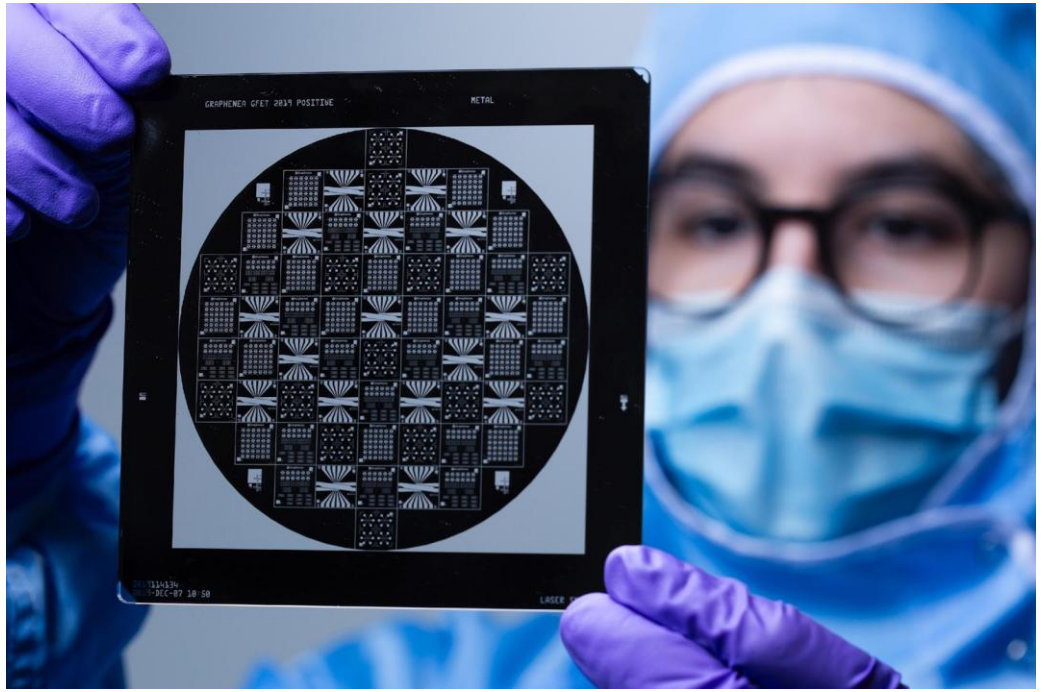
Graphenea

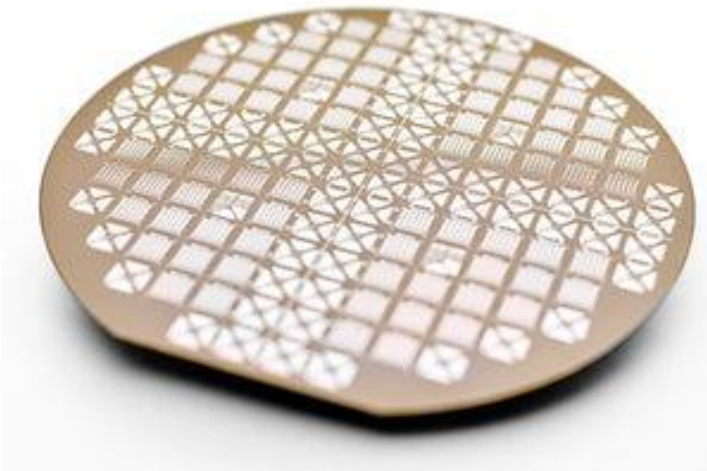
Hands On Training imec
10/02/26



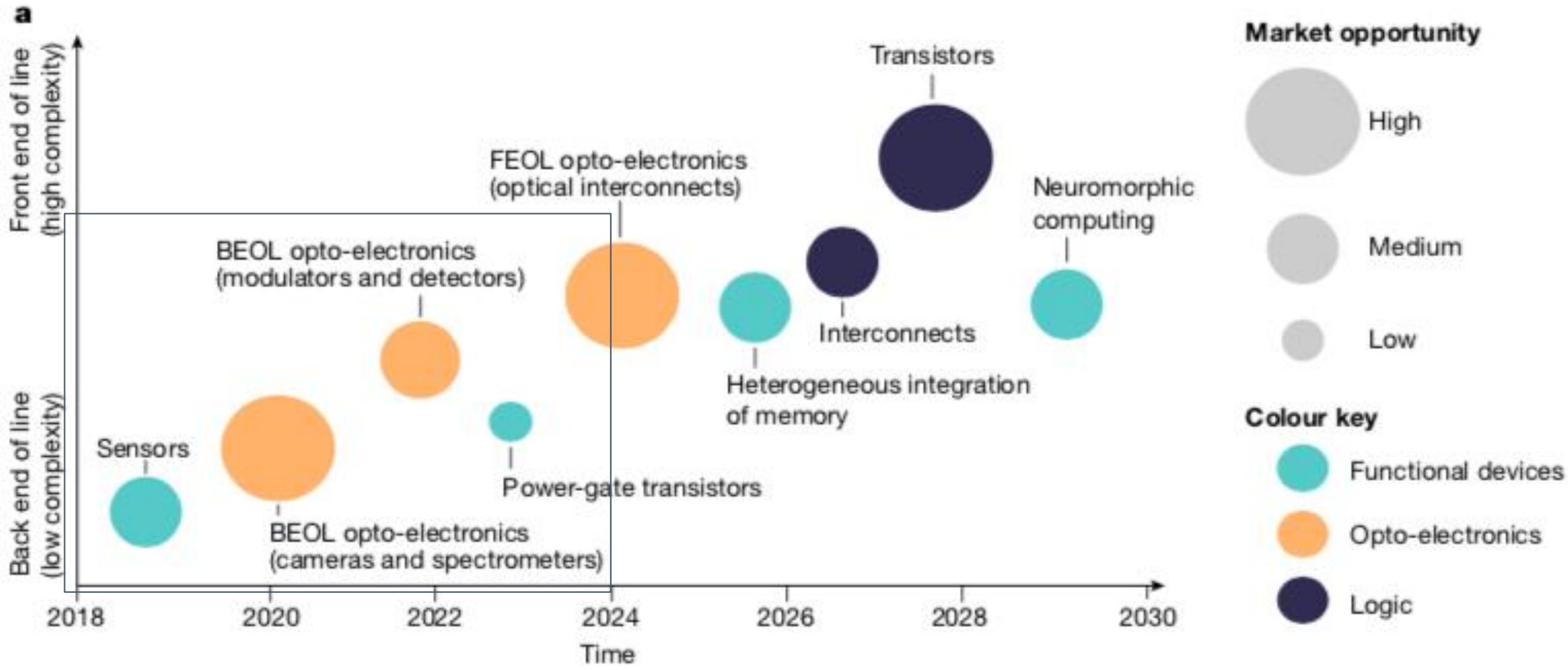
Outline

- Graphene’s state of the art, applications and markets
- PF2 Fabrication steps
- Quality control
- Design rules
- GDS techfile





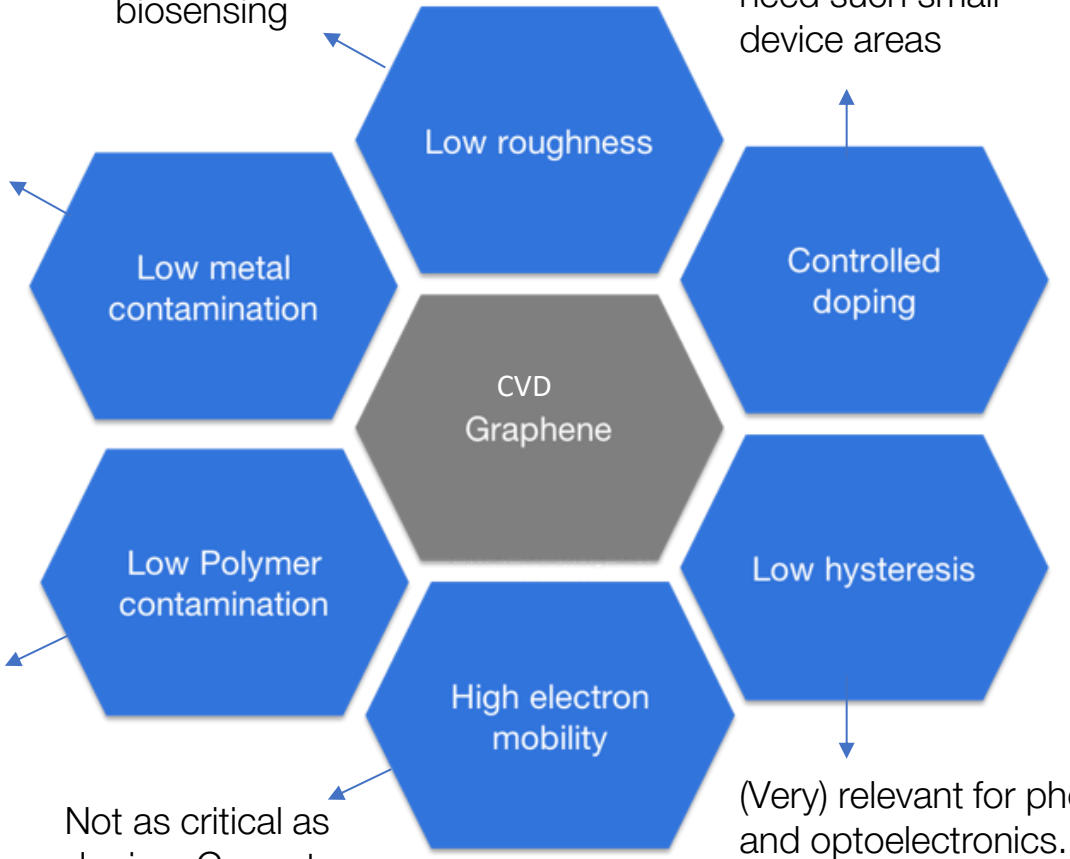
Graphene applications & markets



10.1038/s41586-019-1573-9

Graphene applications & markets

…what do we need?



Roughness can be benefitial for biosensing

Biosensors don't need such small device areas

Dedicated Fabs/Process lines.
BEOL Process

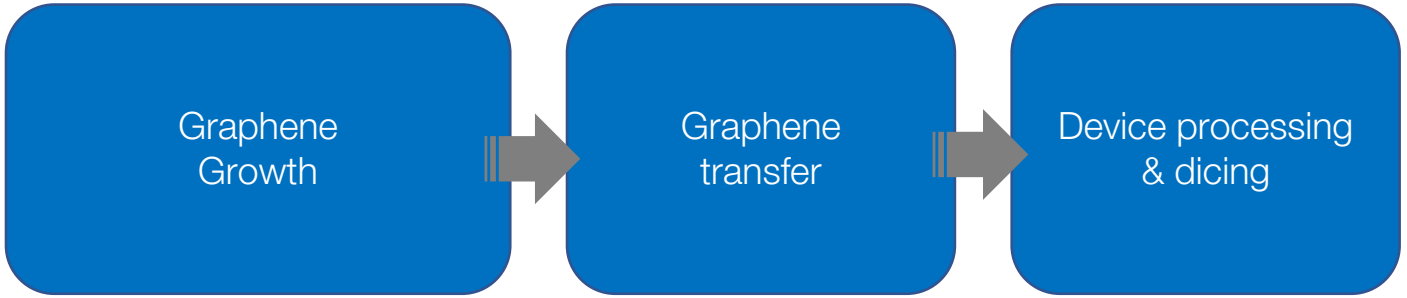
Low doping is critical!
Most applications rely on Fermi level tuning
Reliable functionalization

Not as critical as doping. Current values ≈1000s $cm^2/V{\cdot}s$ are good .

(Very) relevant for photonics and optoelectronics.
May be irrelevant for sensing, or even useful!

Moving from the lab to the fab

Wafer-scale manufacturing processes are critical for its commercial adoption





Graphenea controls all the steps of the manufacturing process: starting from graphene growth which is followed by its transfer and device processing, until they are diced and ready for packaging.

Fabrication steps

Alignment marks

Graphene transfer

Graphene patterning

Contacts metallization

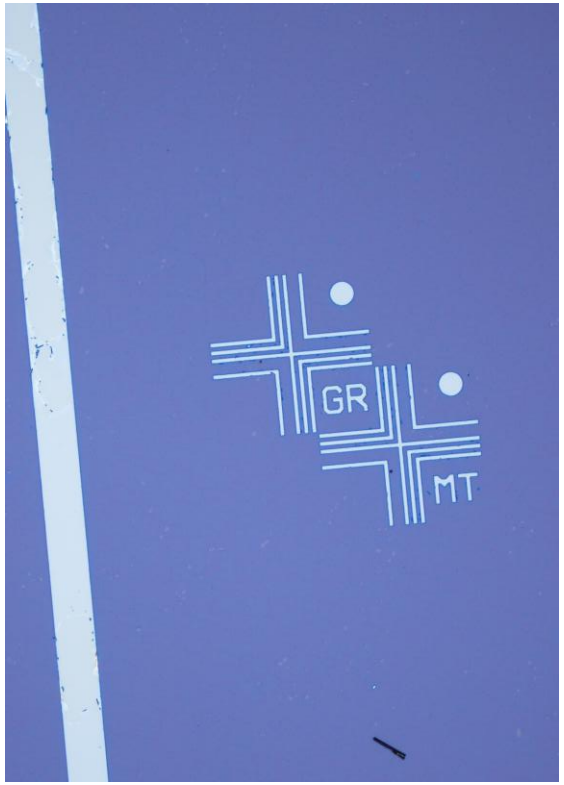
Encapsulation process



S2x device series

Fabrication steps

- Alignment marks

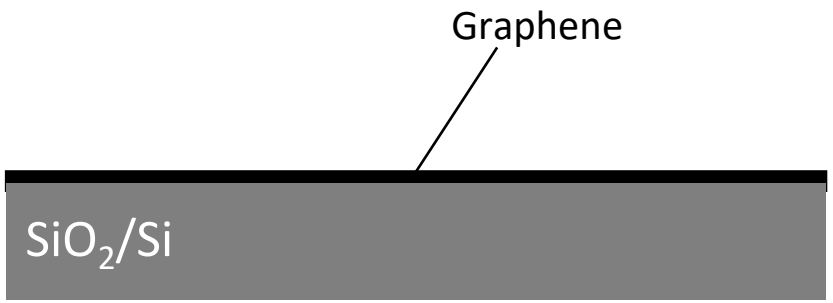




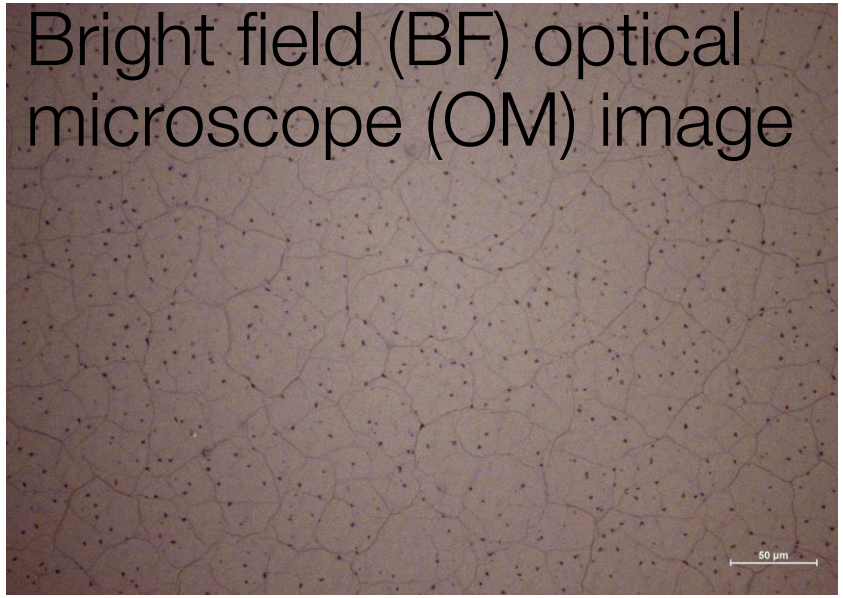
S2x device series

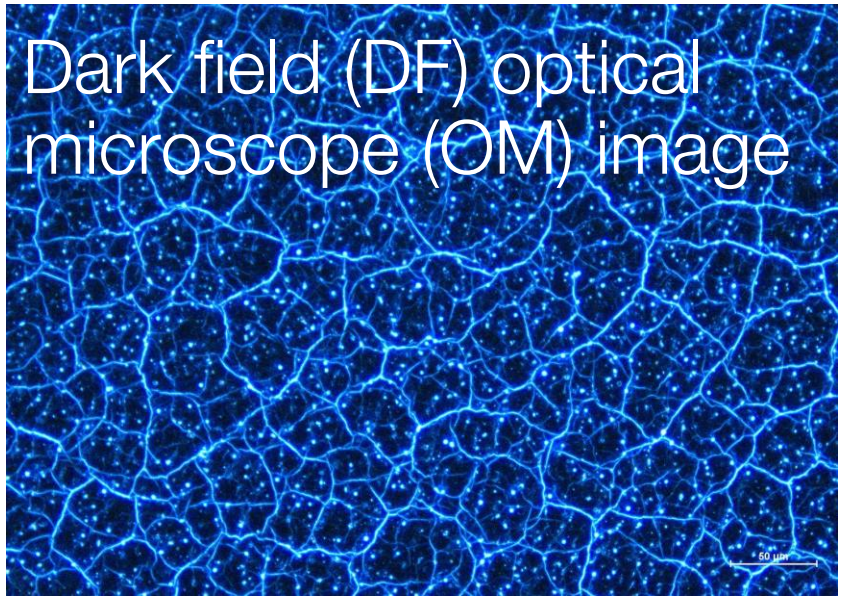
Fabrication steps

➢Graphene transfer



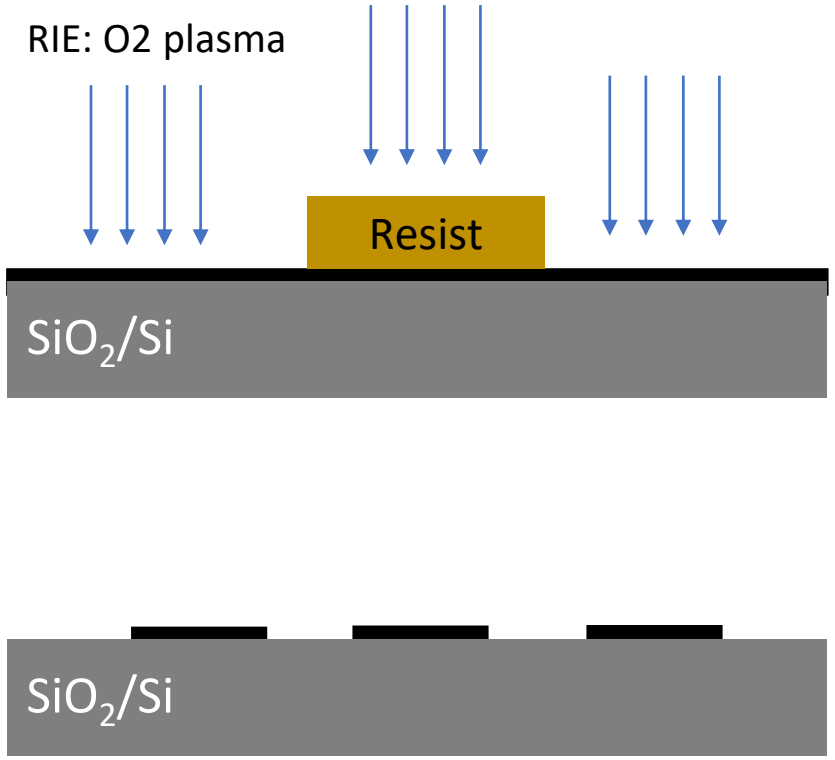


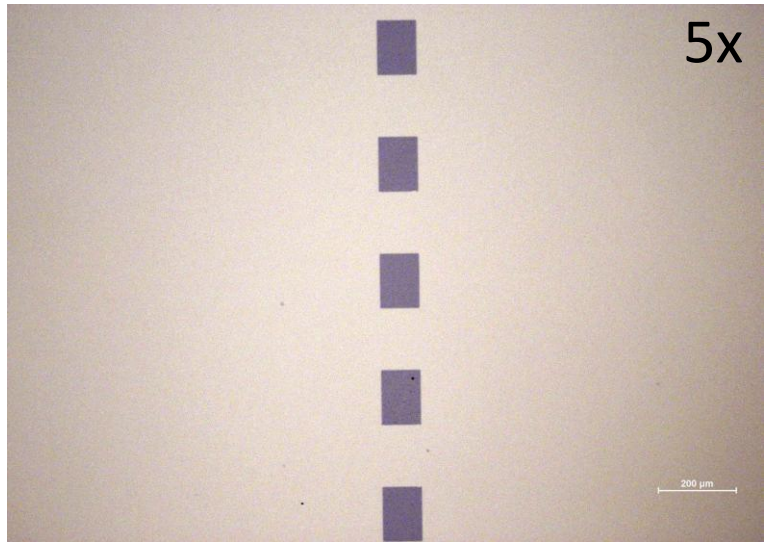


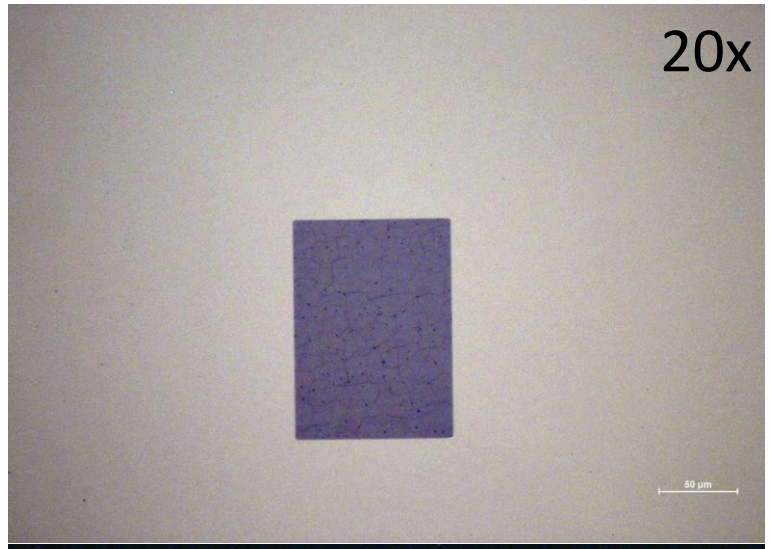


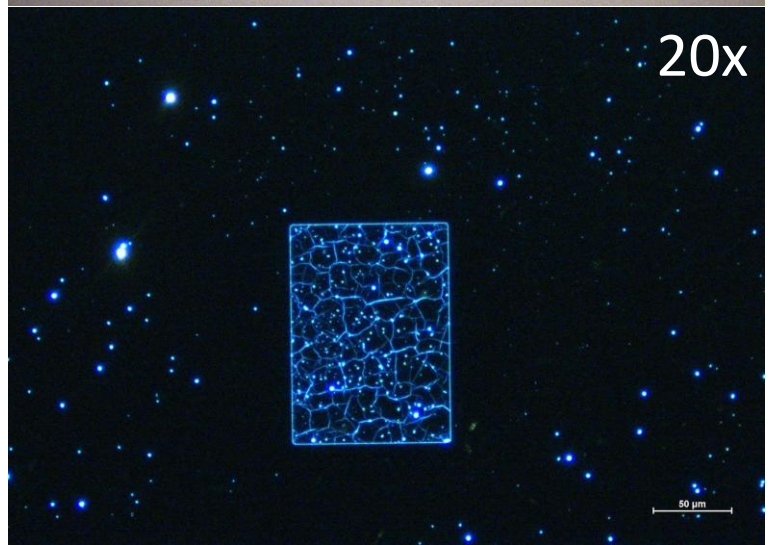
Fabrication steps

➢Graphene patterning: Reactive Ion Etching (RIE)



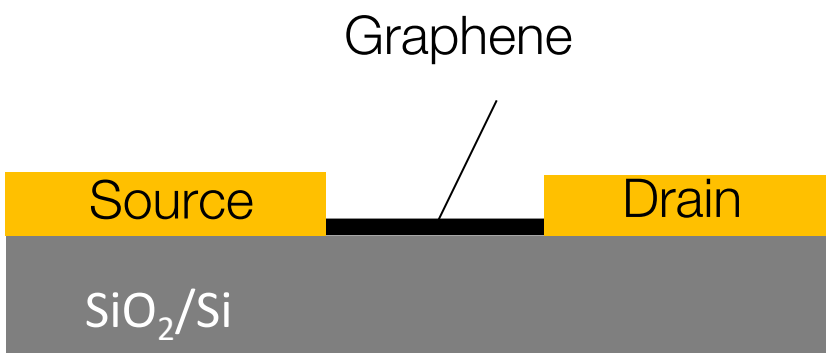


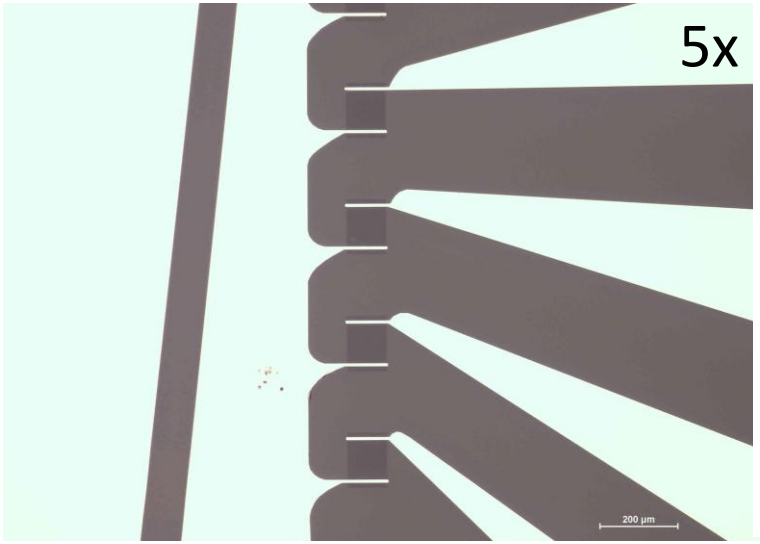


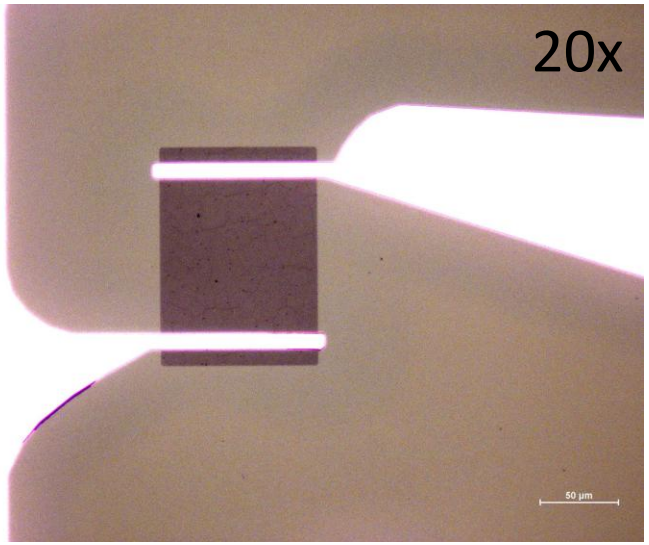


Fabrication steps

➢Contacts metallization

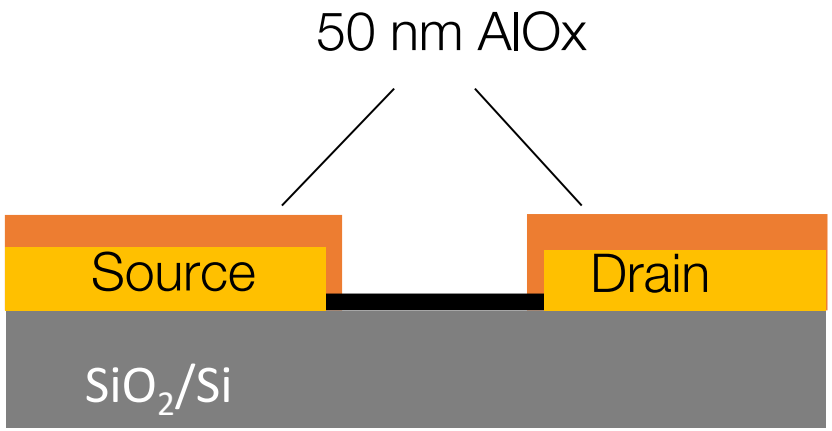


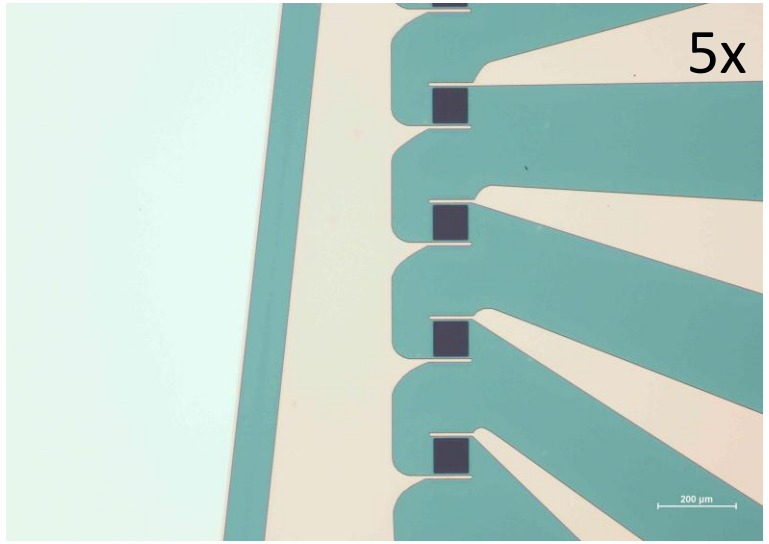


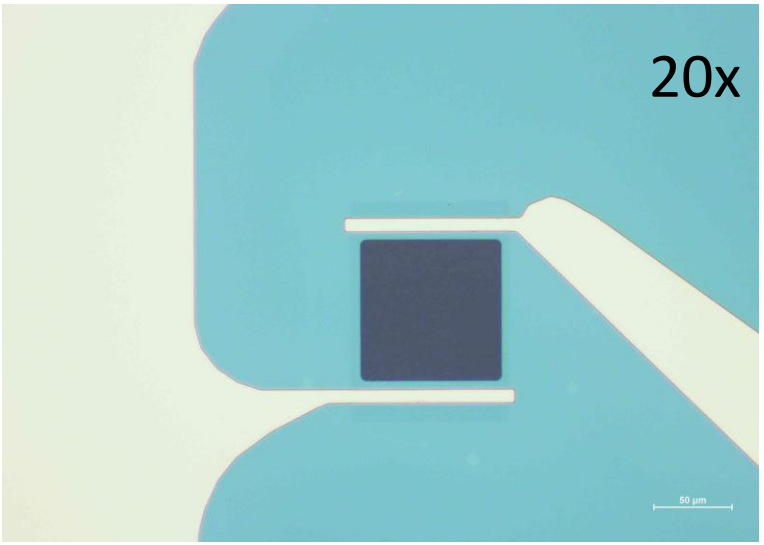


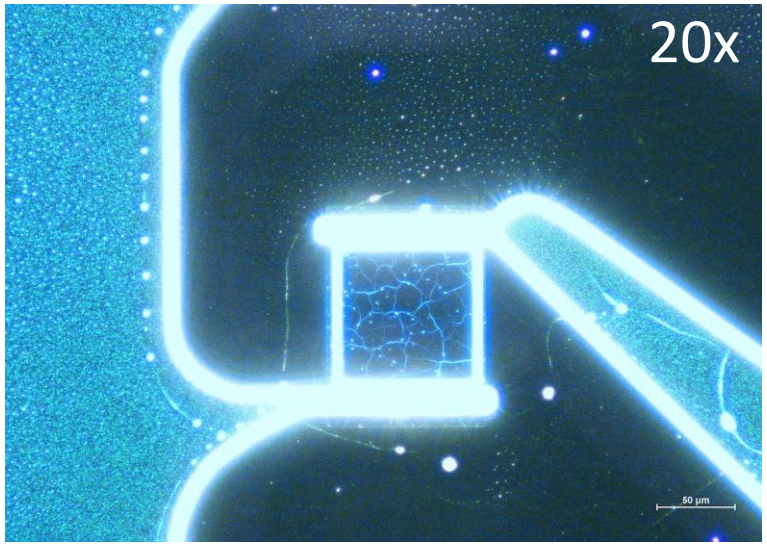
Fabrication steps

➢Encapsulation process: 50 nm AlOx



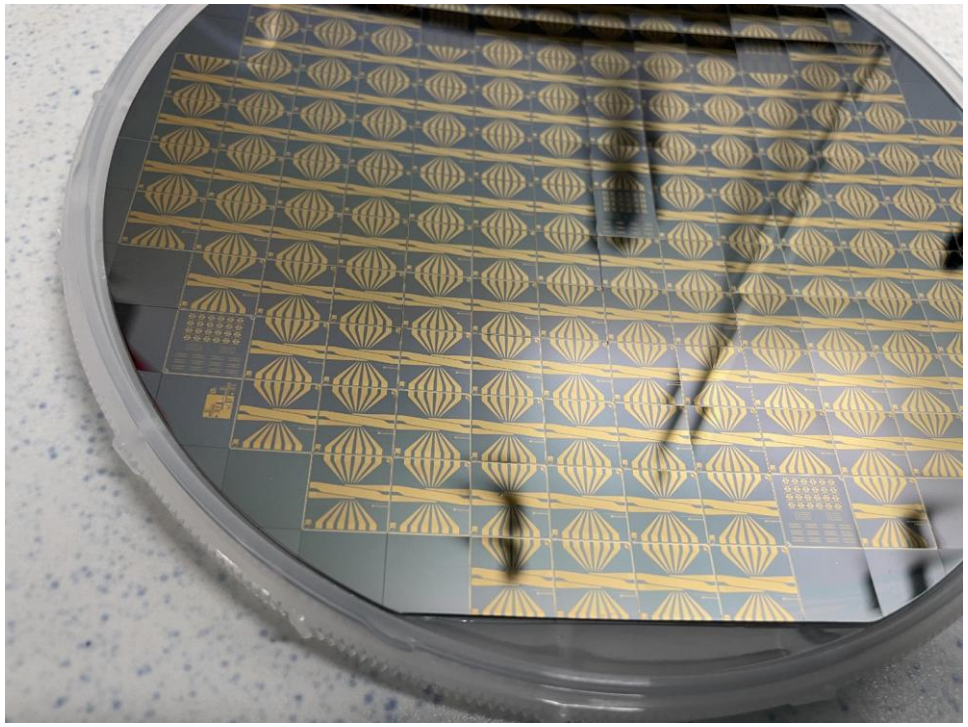


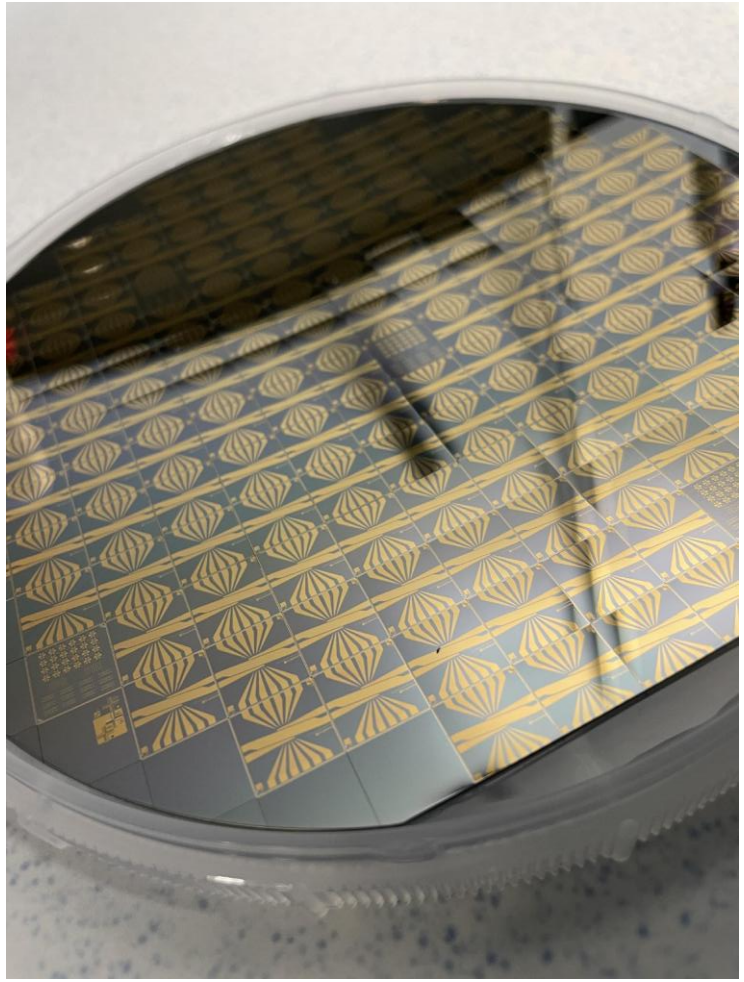




Fabrication steps

- Dicing





Graphenea Quality control

ISO 9001:2015
ISO 13485:2016

A complete in-line inspection is key to achieve good manufacturing standards and reliability

Graphene Growth → Graphene transfer → Device processing & dicing

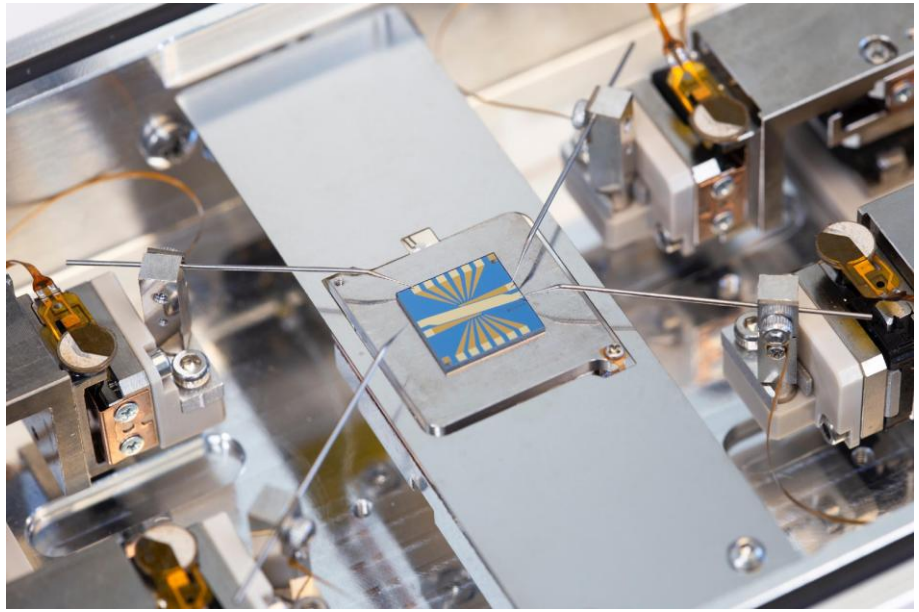


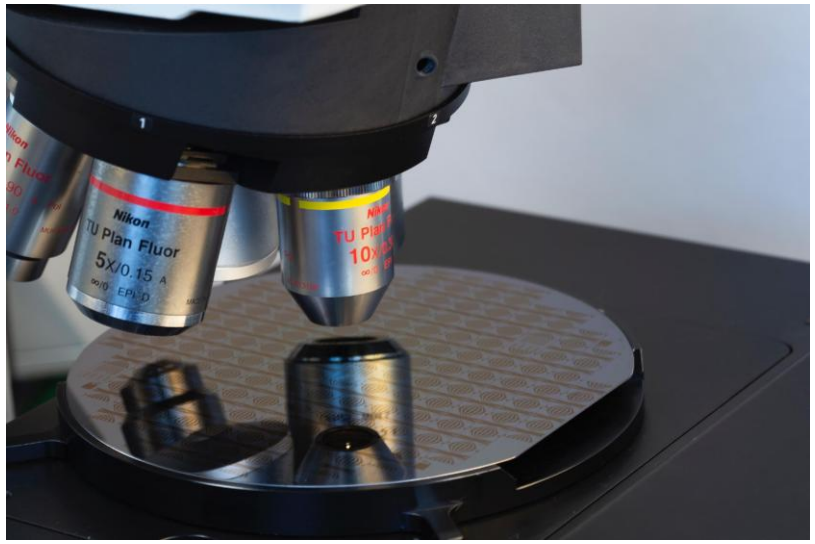
Optical, AFM, Raman and Electrical

Private and confidential

Quality control

- Optical microscope: channel integrity > 95% and device yield > 75%
- Transport characterization: Mobility, Dirac point and hysteresis measurements

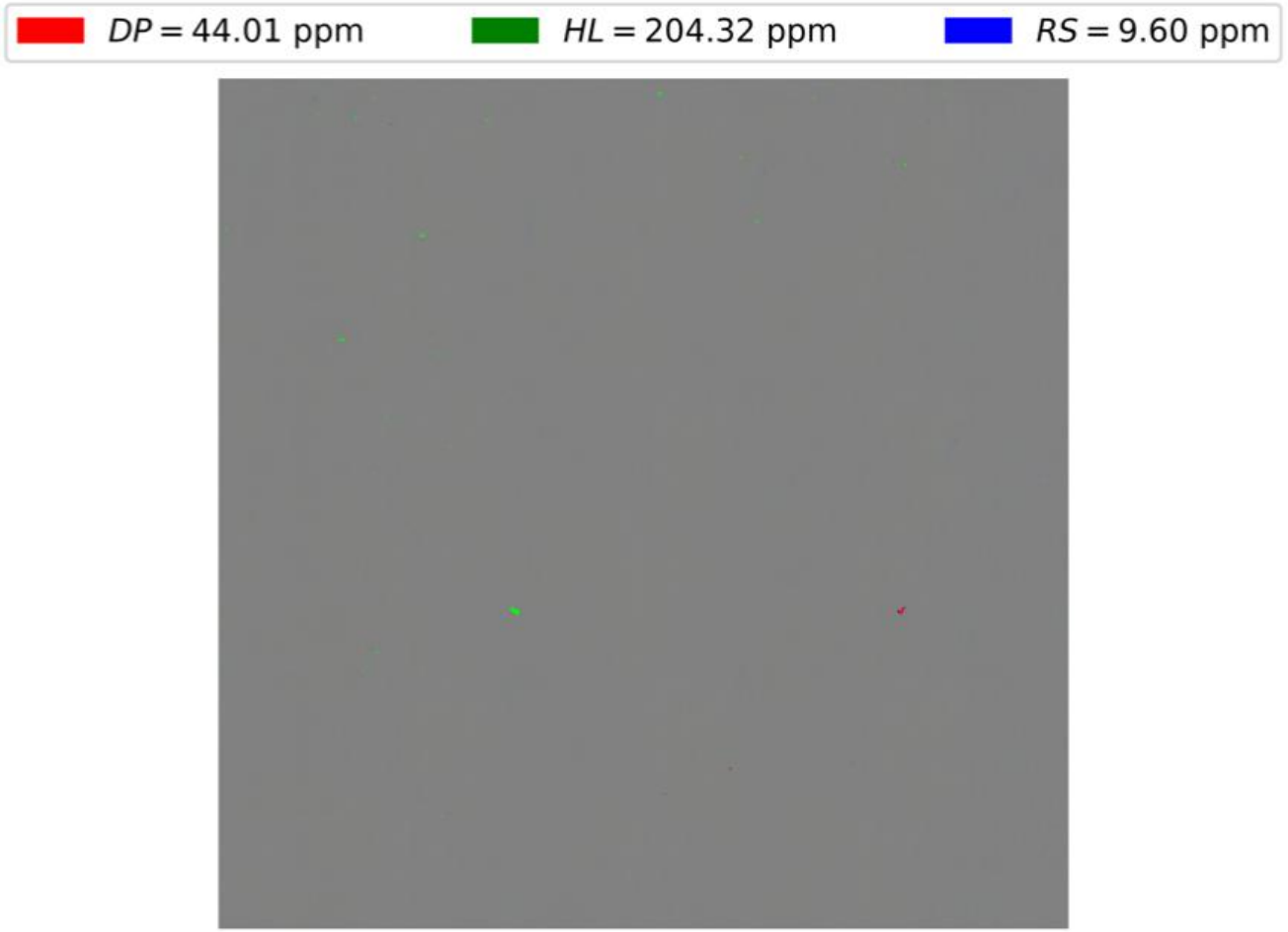


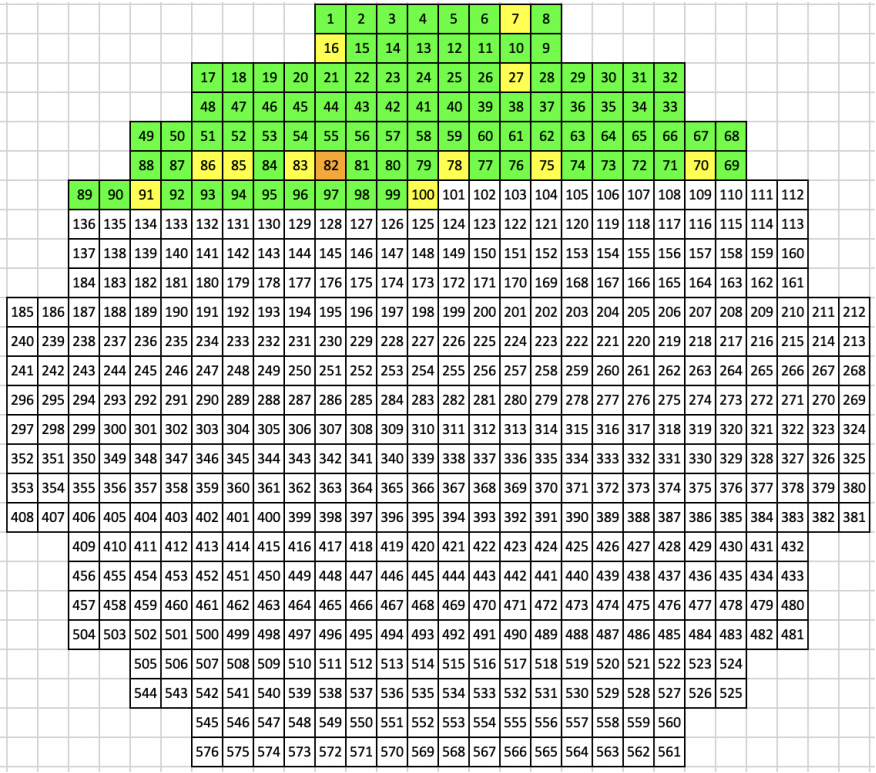


- AFM: RMS and Ra roughness
- Raman: I(G)/I(2D) and I(D)/I(G) ratios, G position < 1600 cm^{-1} and FWHM (2D) < 45 cm^{-1}

Quality control – Before fabrication

- Optical microscope: pictures are fed into an algorithm that distinguishes between holes, particles and polymeric residues for statistical analysis

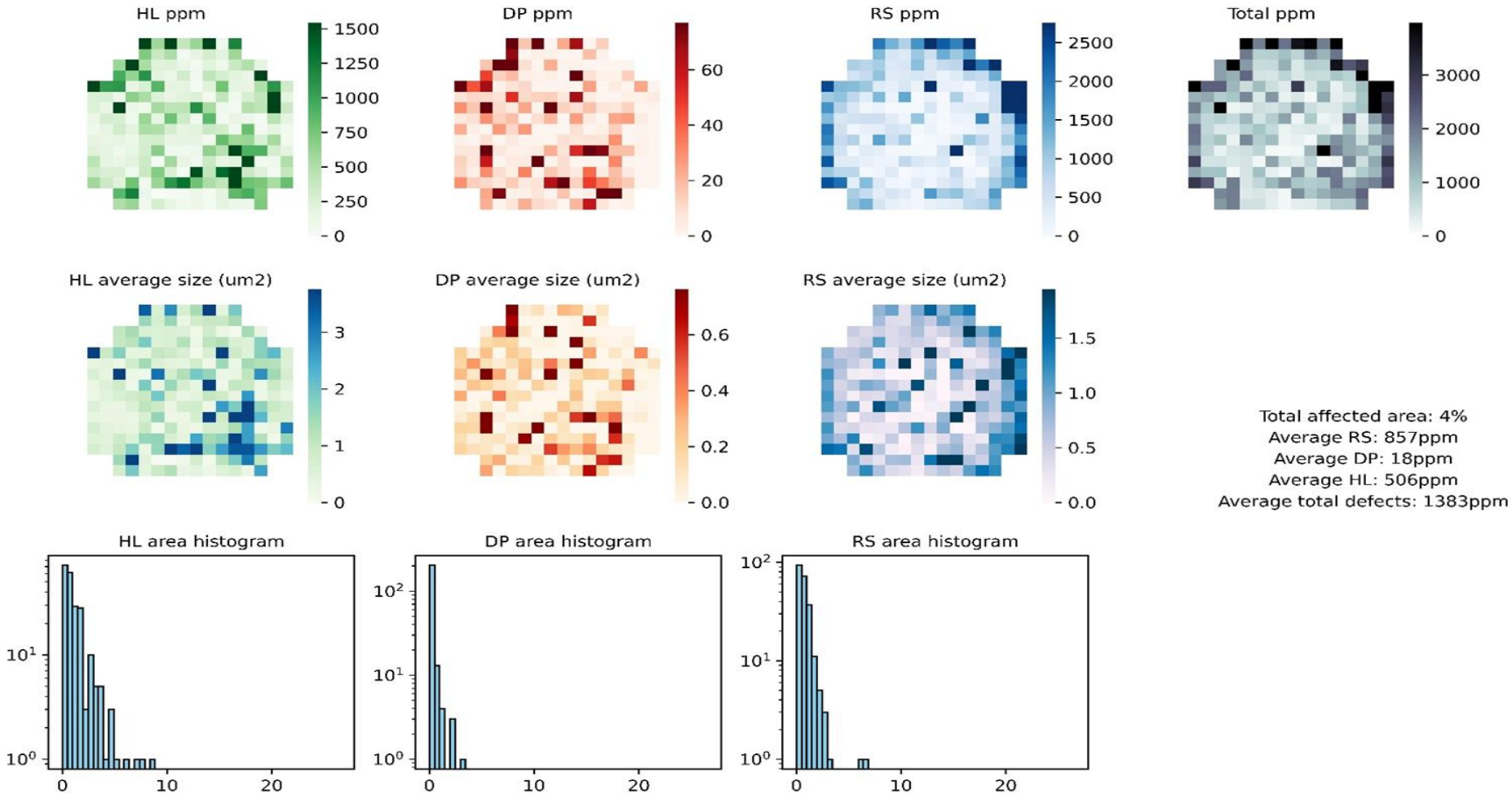




Quality control – Before fabrication

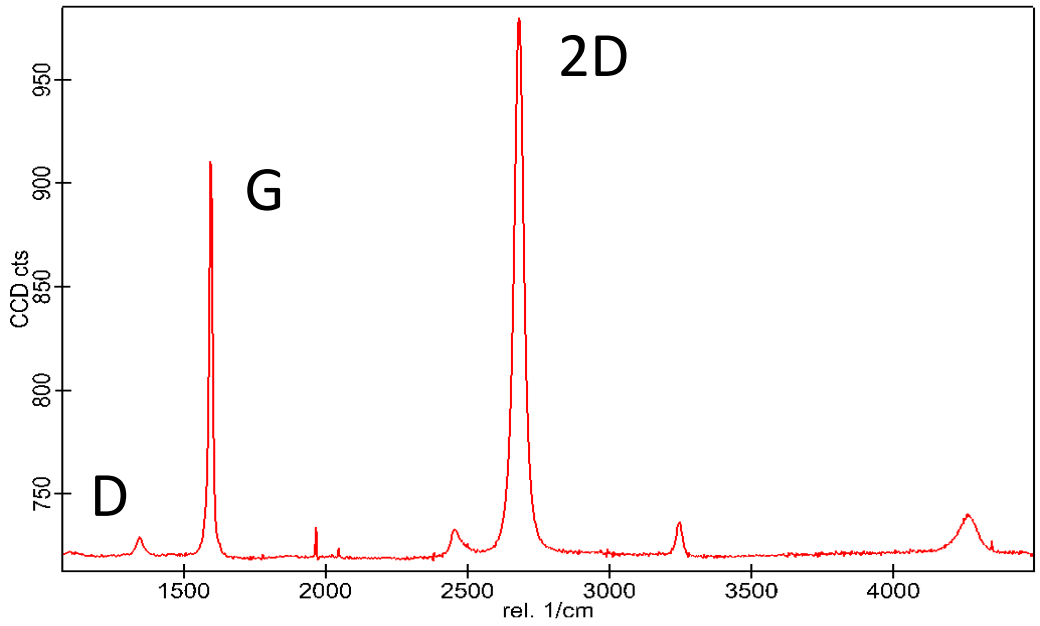
- Optical microscope:

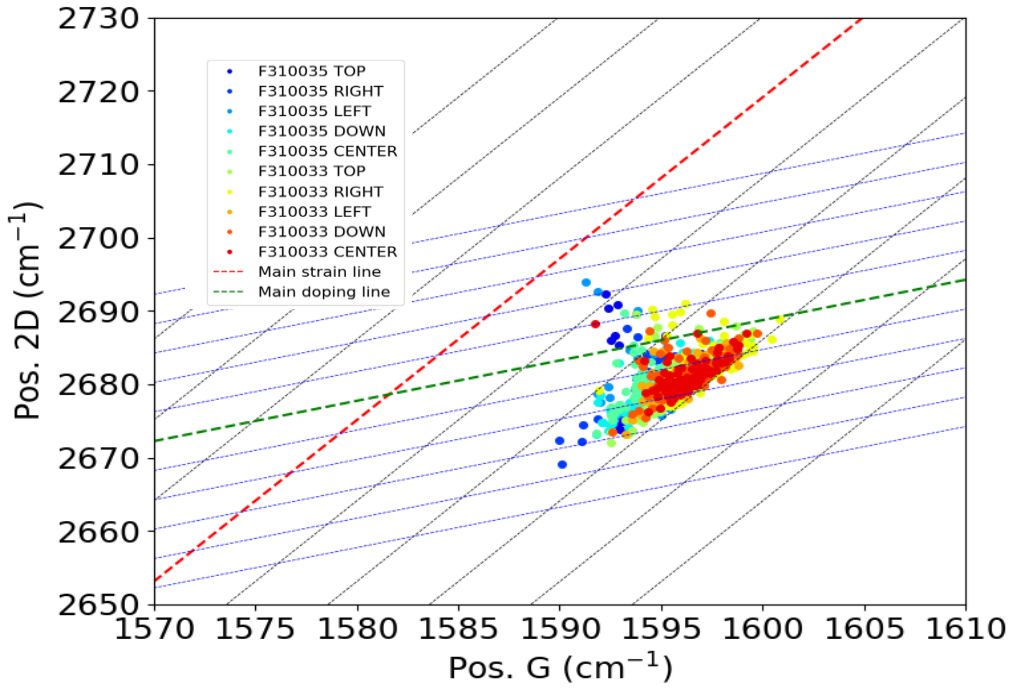
Quality **A** / Total affected area 4%



Quality control – Before fabrication

- Raman:





Sample	Data	Frequency D (cm-1)	Frequency G (cm-1)	FWHM G (cm-1)	Frequency 2D (cm-1)	FWHM 2D (cm-1)	ID/IG	IG/I2D
FXXXXX	Avg	1345	1596	13	2681	39	0.05	0.75
	St. Dev	5	1	1	3	2	0.02	0.05

✓ Pos(G) < 1600 cm^{-1}

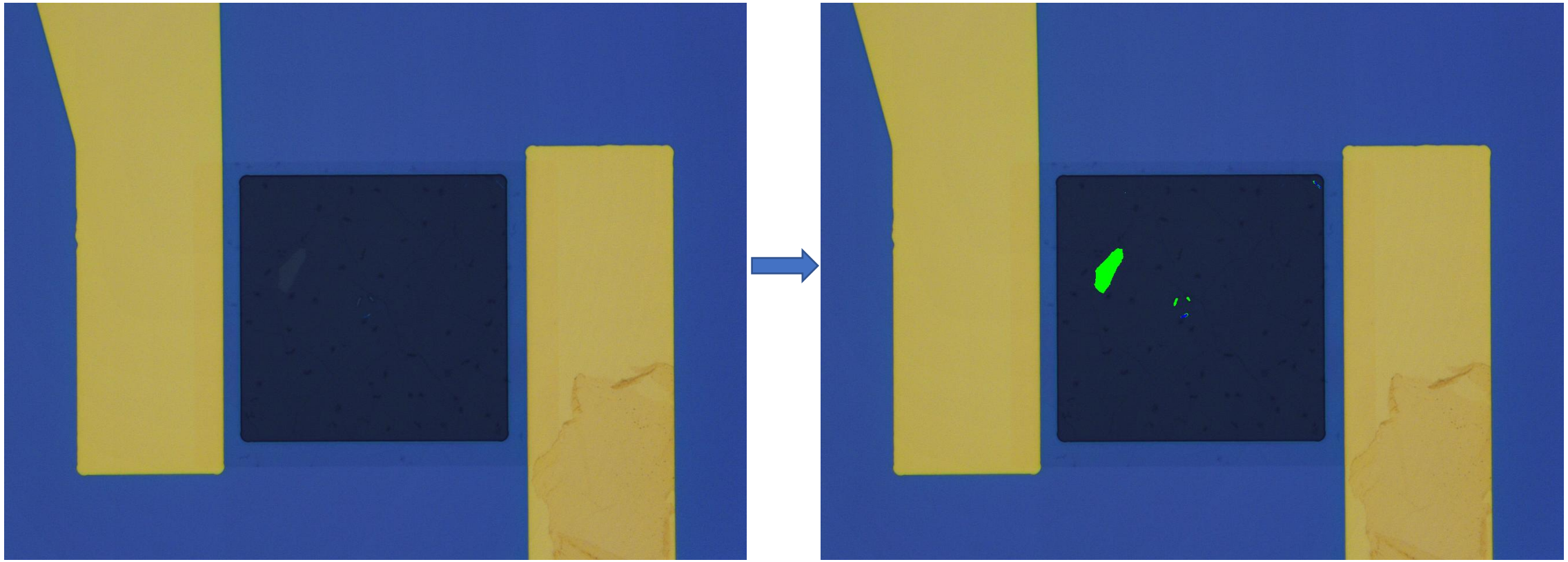
✓ FWHM(2D) < 45 cm^{-1}

✓ I(G)/I(2D) < 1.25

✓ I(D)/I(G) < 0.15

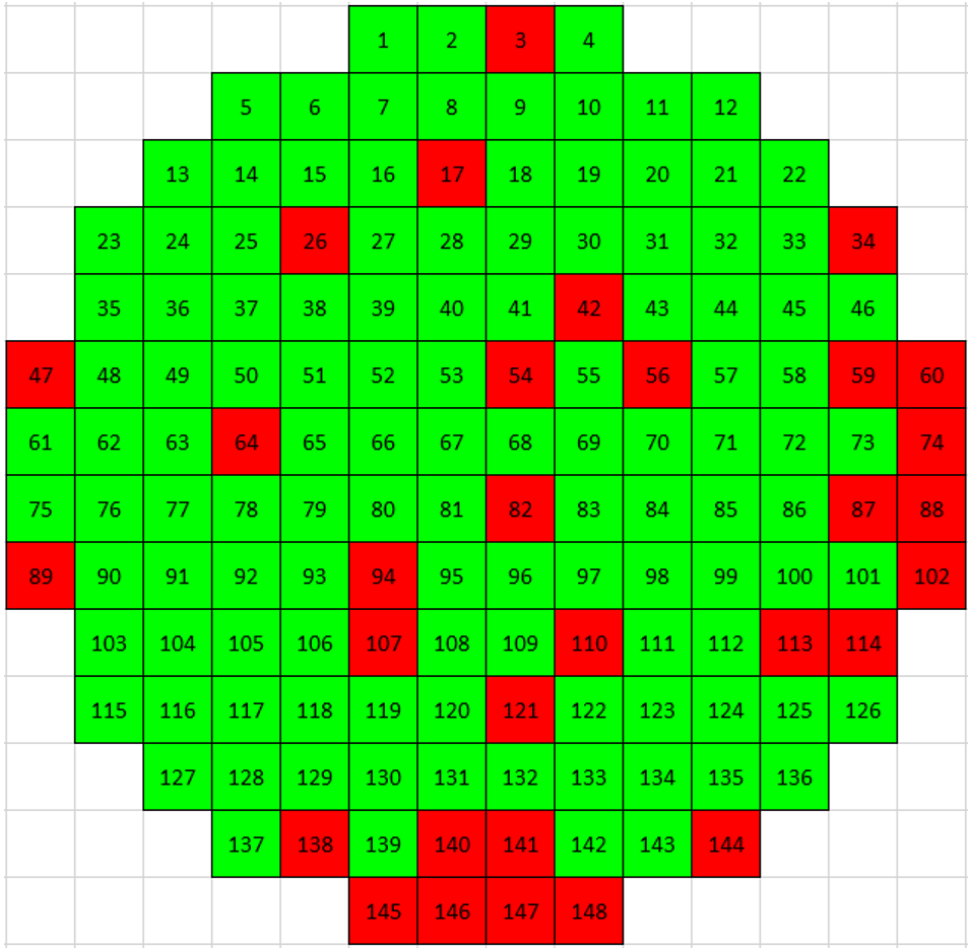
Quality control – After fabrication

- Optical microscope: pictures are fed into an algorithm that distinguishes between holes, particles and polymeric residues for statistical analysis



Quality control – After fabrication

- Optical microscope: holes, particles and polymeric residues

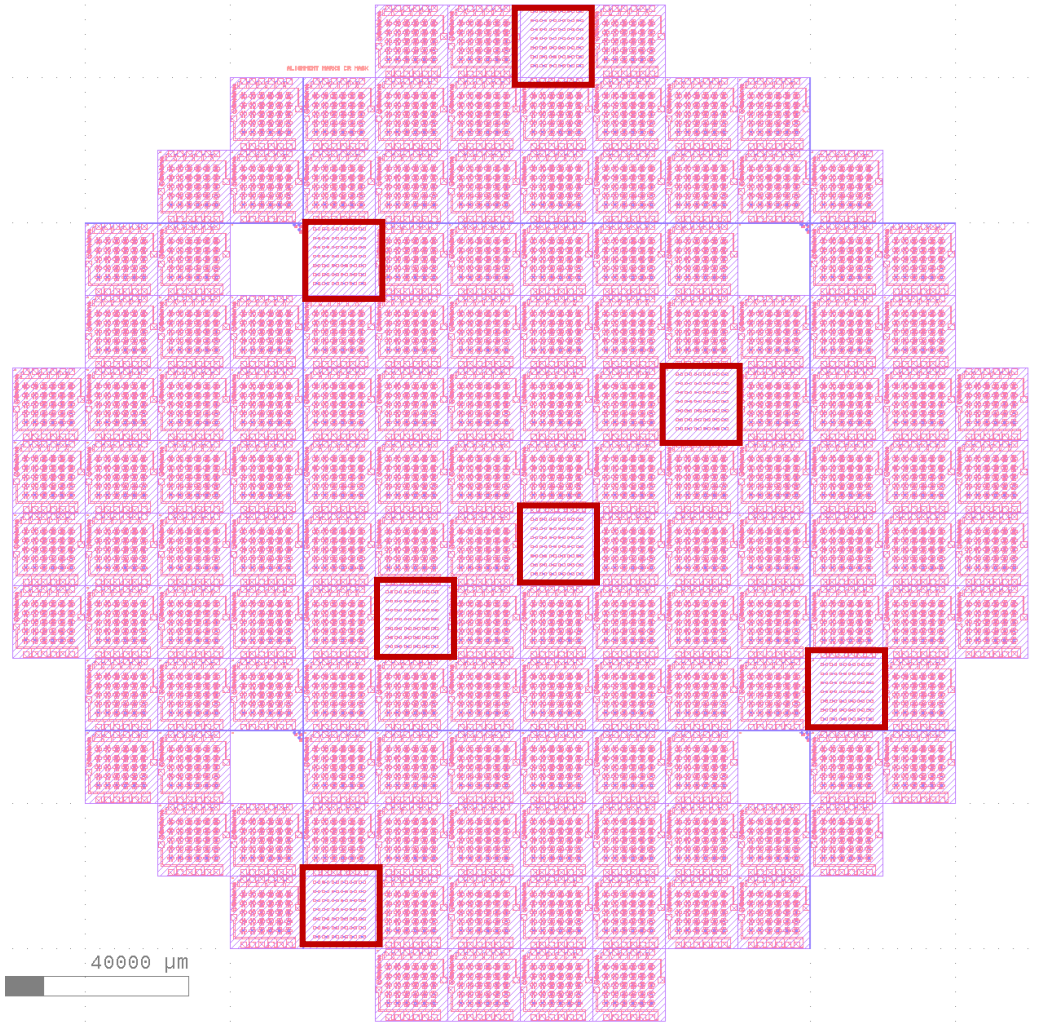


✓ Channel integrity > 95%

✓ Device yield > 75%

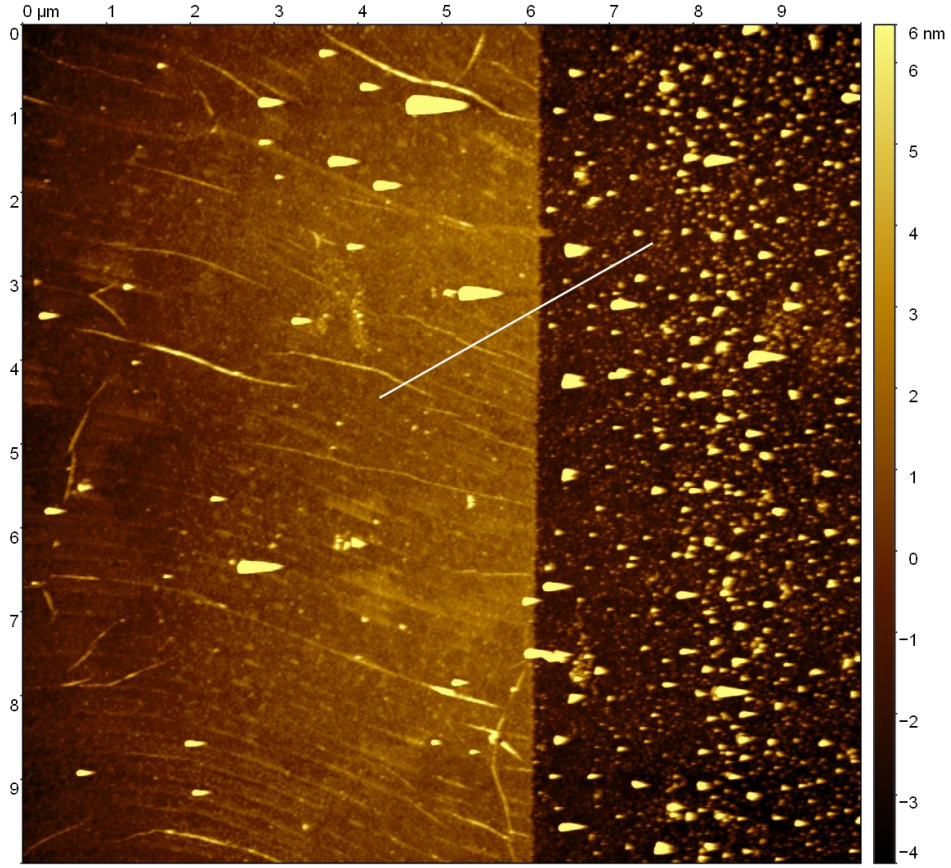
Quality control – After fabrication in PCM dies

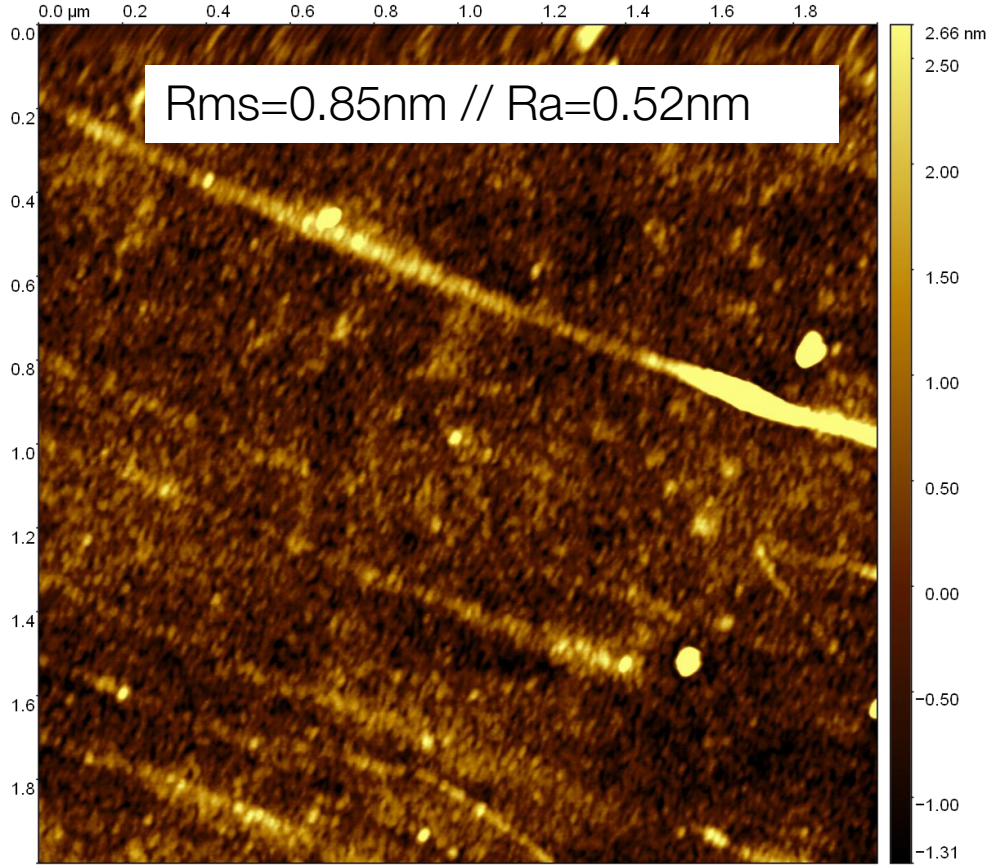
- Process Control Monitor (PCM) dies: AFM, Raman, transport measurements



Quality control – After fabrication in PCM dies

- AFM: Roughness Average (Ra) and Root Mean Square (RMS)



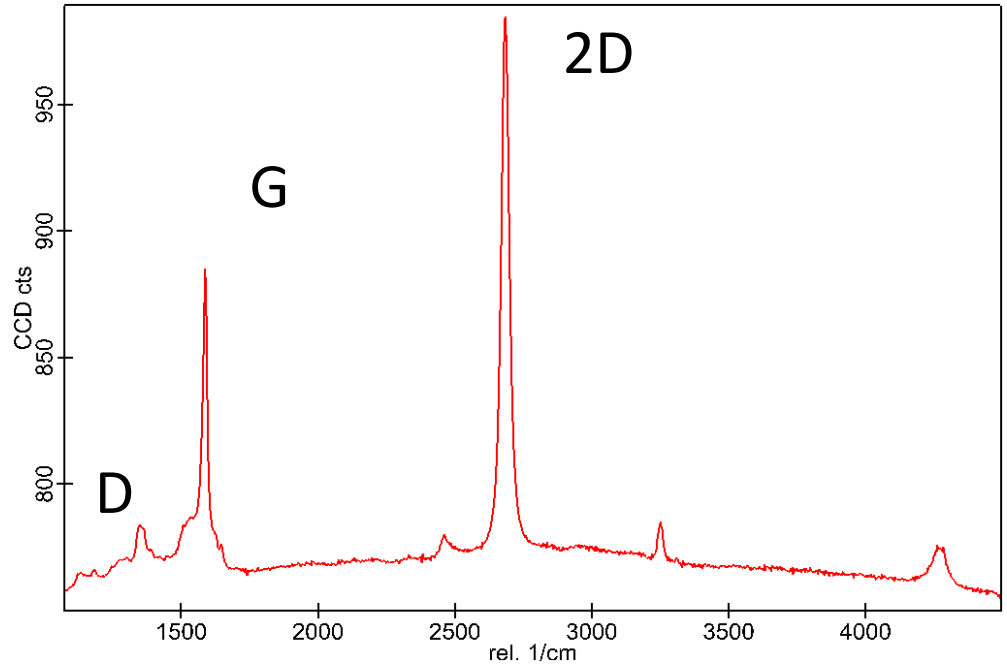


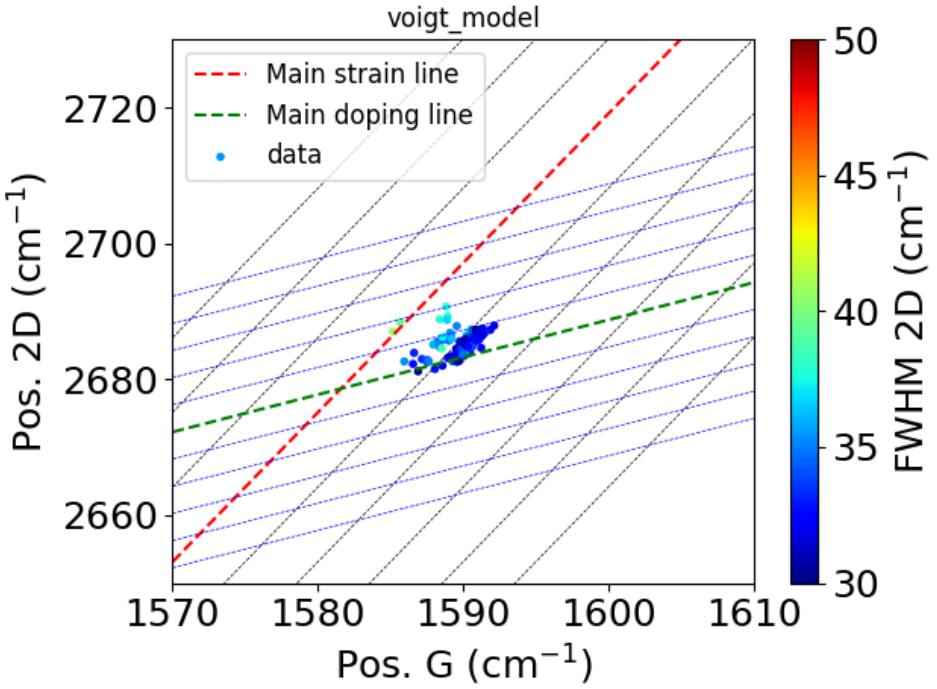
✓ RMS < 1.5 nm

✓ Ra < 1.0 nm

Quality control – After fabrication in PCM dies

- Raman:





Sample	Frequency D (cm-1)	Frequency G (cm-1)	FWHM G (cm-1)	Frequency 2D (cm-1)	FWHM 2D (cm-1)	ID/IG	IG/I2D
Avg	1354	1587	17	2684	34	0.15	0.51
St. Dev	6	2	5	2	2	0.06	0.14

✓ Pos(G) < 1600 cm^{-1}

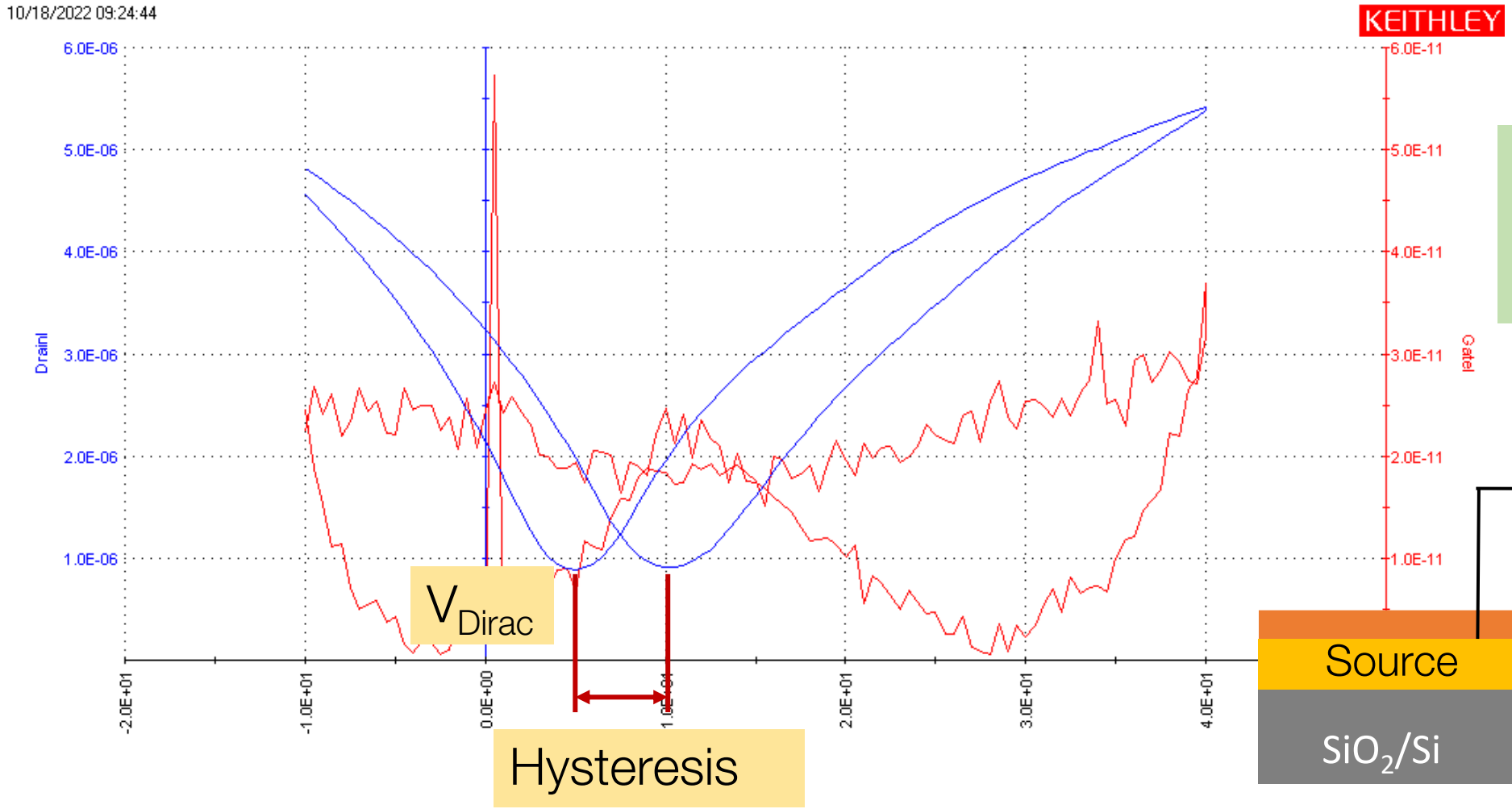
✓ FWHM(2D) < 45 cm^{-1}

✓ I(G)/I(2D) < 1.25

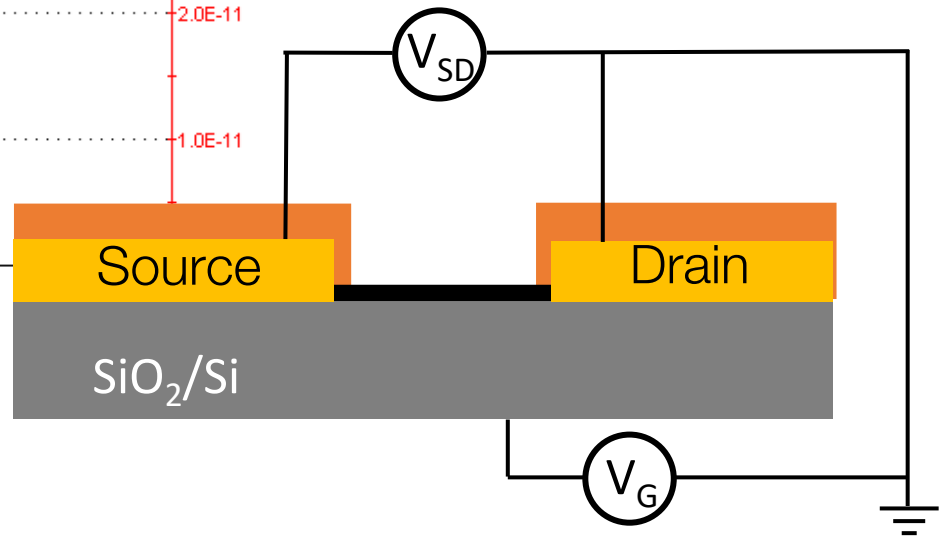
✓ I(D)/I(G) < 0.15

Quality control – After fabrication in PCM dies

- Transport characterization: mobility, Dirac point and hysteresis measurements

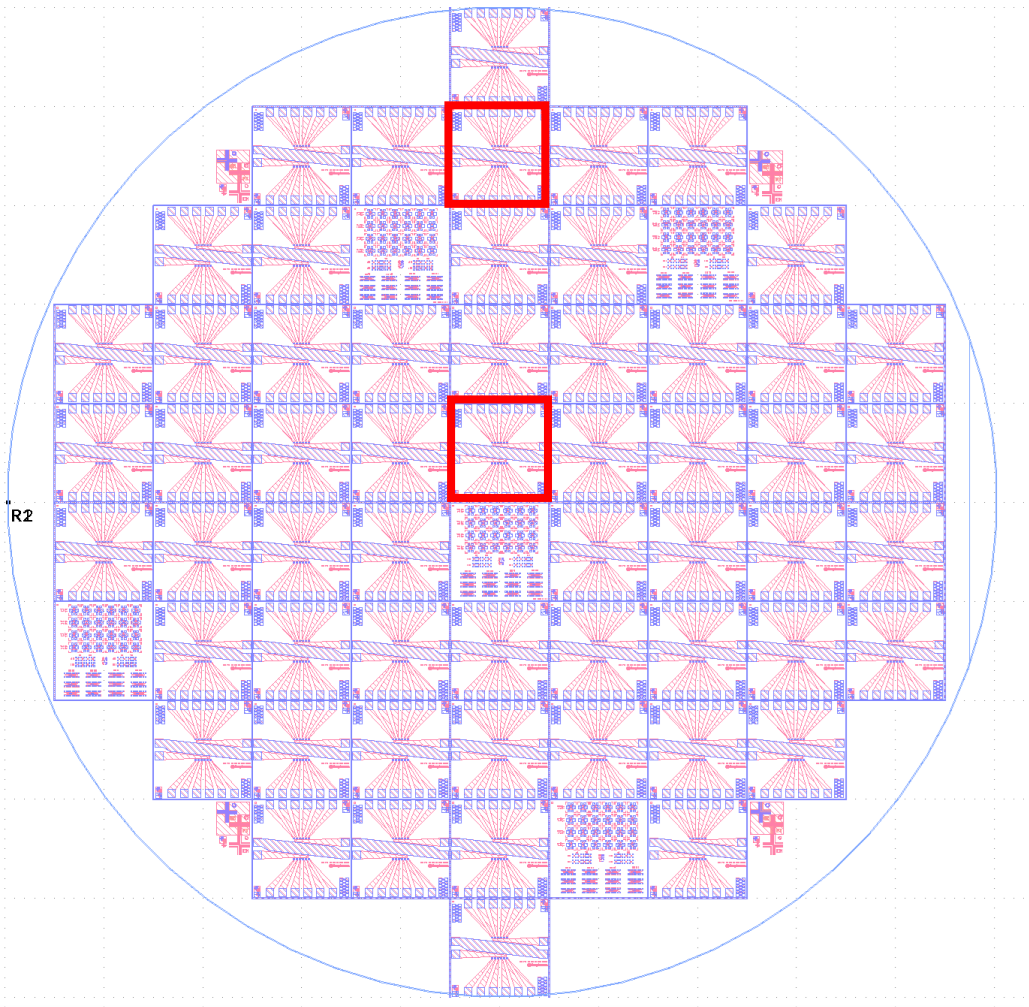


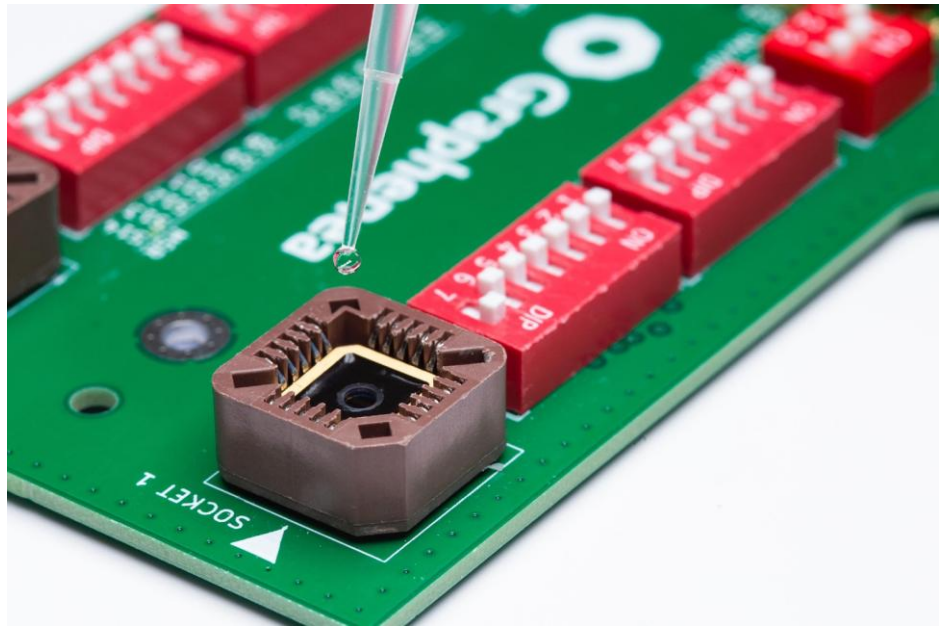
- ✓ V_{Dirac} < 20 V
- ✓ Hysteresis < 10 V
- ✓ Mobility > 1000 $cm^2/V{\cdot}s$



Quality control – After fabrication in PCM dies

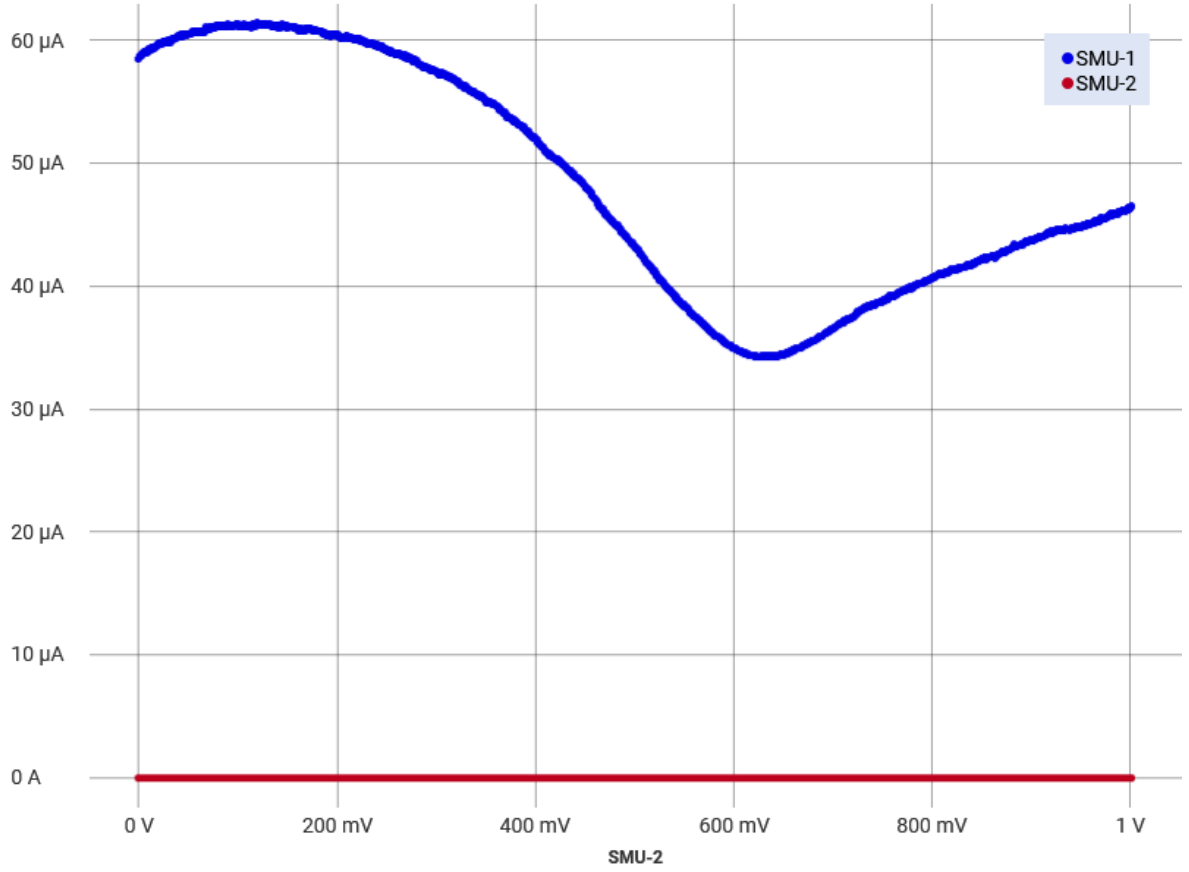
- Liquid gating measurements





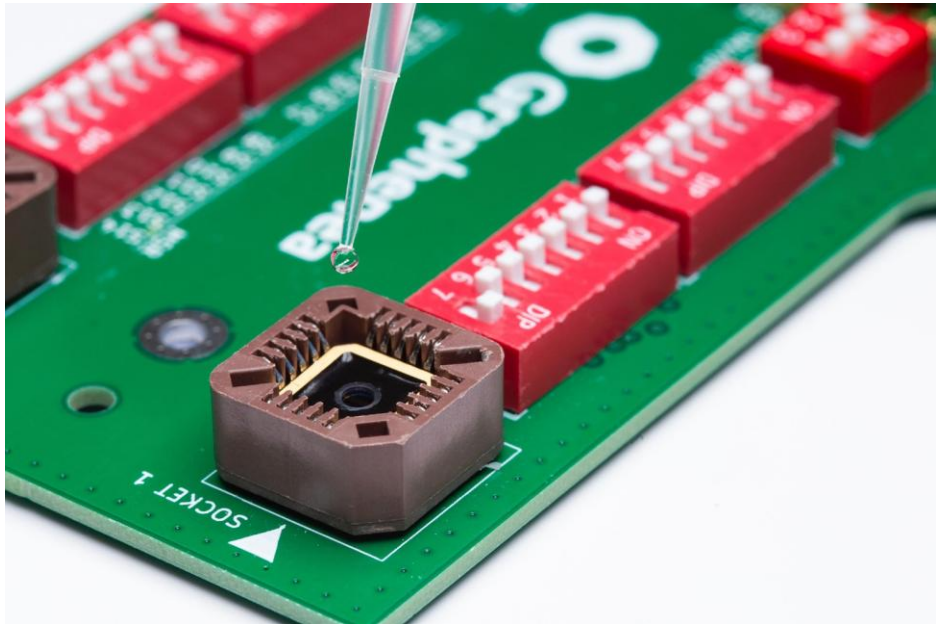
Quality control – After fabrication in PCM dies

- Liquid gating measurements



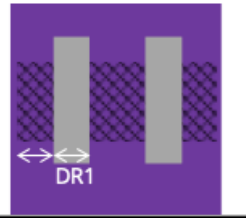
S20 example	Dirac Point (V)
Avg	0.62
Median	0.62
Std	0.02

✓ Average Dirac point with liquid gating < 1 V

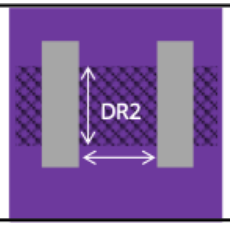


Design rules

Design rules

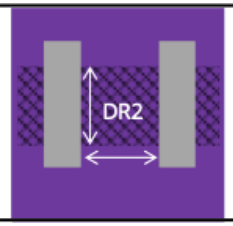
DR1	Minimum feature size – metal	10 µm	

- Resist left-overs/ lithography definition
- Because alignment reasons

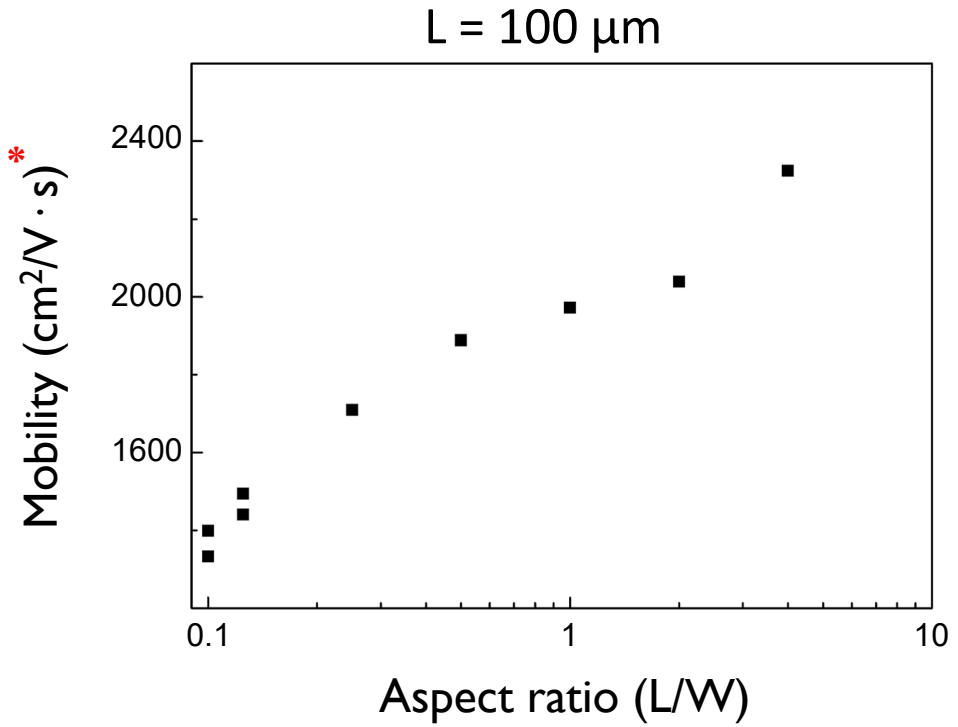
DR2	Minimum feature size – graphene	65 µm	

- This design rule directly connects with the encapsulation one (DR7)

Design rules

DR2	Minimum feature size – graphene	65 µm	

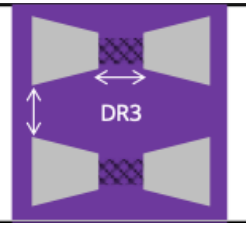
➢ Lithography definition



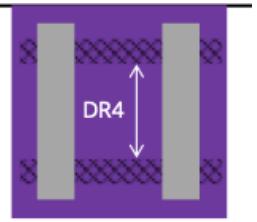
Device width (µm)	L/W
65 - 100	>2
>100	>1

* Data from PCM dies of Process Flow I

Design rules

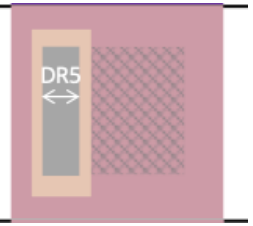
DR3	Minimum feature separation – metal	50 µm	

- Due to lift-off reasons to ensure high yield

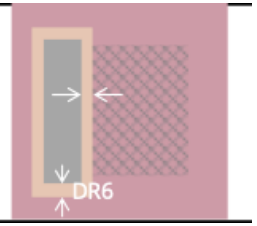
DR4	Minimum feature separation - graphene	20 µm	

- Due to definition reasons

Design rules

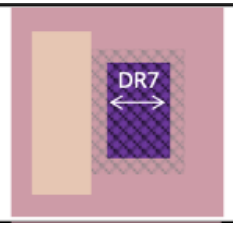
DR5	Minimum via opening size – metal	25 µm	

➢ For avoiding encapsulation opening issues

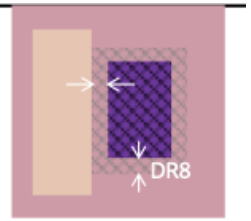
DR6	Minimum via opening to metal edge distance	10 µm	

➢ Lithography alignments

Design rules

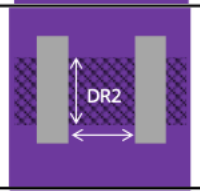
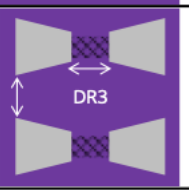
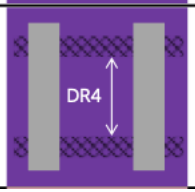
DR7	Minimum via opening size – Graphene	25 µm	

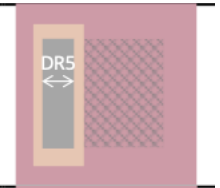
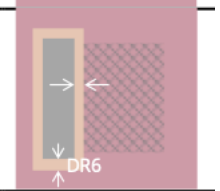
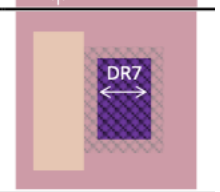
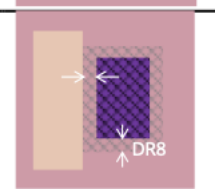
- For avoiding encapsulation opening issues

DR8	Minimum via opening to graphene edge distance	10 µm	

- Lithography alignments

Design rules

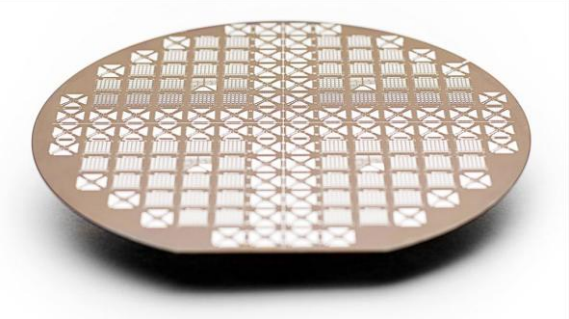
DR1	Minimum feature size – metal	10 µm	
DR2	Minimum feature size – graphene	65 µm	
DR3	Minimum feature separation – metal	50 µm	
DR4	Minimum feature separation - graphene	20 µm	

DR5	Minimum via opening size – metal	25 µm	
DR6	Minimum via opening to metal edge distance	10 µm	
DR7	Minimum via opening size – Graphene	25 µm	
DR8	Minimum via opening to graphene edge distance	10 µm	

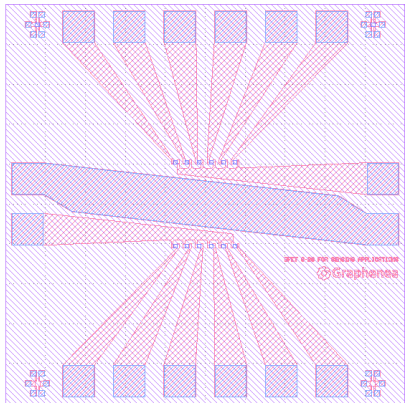
Reducing costs: economy of scale

- Processing steps don't limit the final device cost. The $/chip is determined by its footprint, not by the amount of features
- More dramatic in graphene as its processing is relatively simple (10-50 processing steps) compared with Si (100-1000s processing steps)

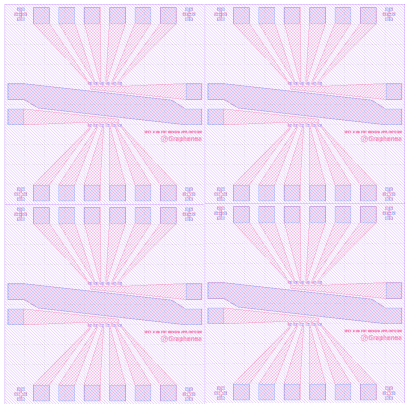
- Substrate cost is almost negligible. The choice of substrate is determined by application or form-factor, not by cost.



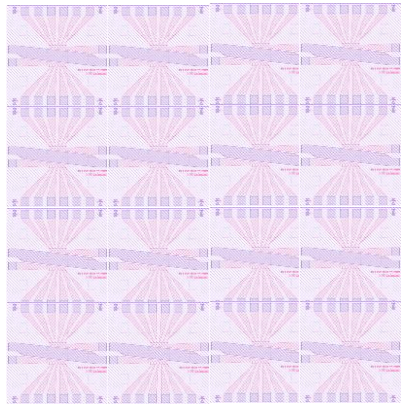
16x cost/chip reduction



4x



4x



10x10 mm^2
≈60 chips in 100mm wafer

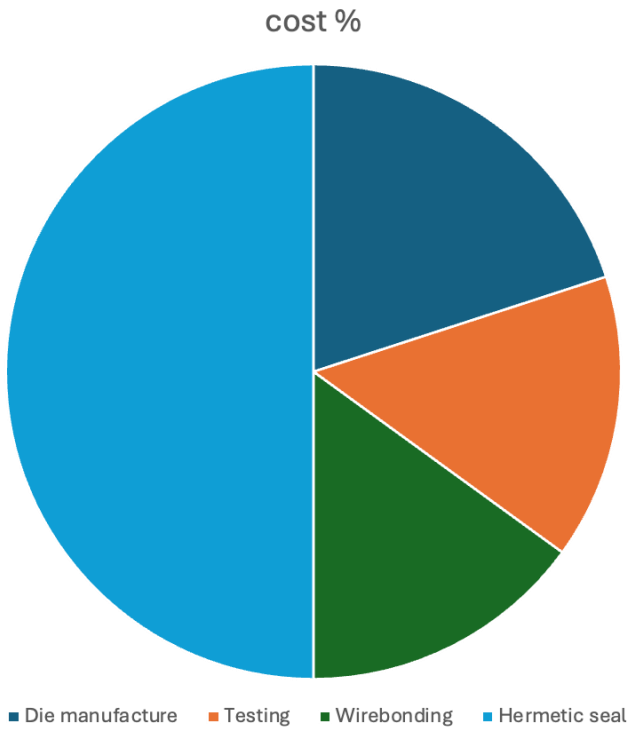
5x5 mm^2
≈250 chips in 100mm wafer

2.5x2.5 mm^2
≈1000 chips in 100mm wafer

Graphenea

Design with packaging in mind

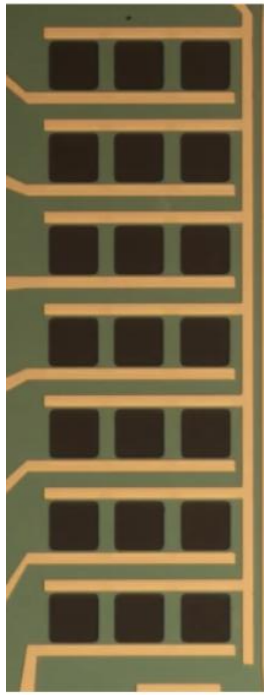
- Ultimately, the cost of the final product will be dominated by the cost of the packaging.
- More dramatic in graphene as its processing is relatively simple (10-50 processing steps) compared with Si (100-1000s processing steps)
- The packaging process/approach (LCC vs PCB, wirebonding vs printed electrodes, microfluidics..) has a major impact on final price.



Graphenea

Design with multiplexing in mind

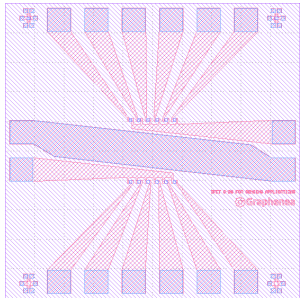
- Type of functionalization (antibodies, aptamers, nanoparticles..) and number of targets have large impact on not only device form factor but product form factor

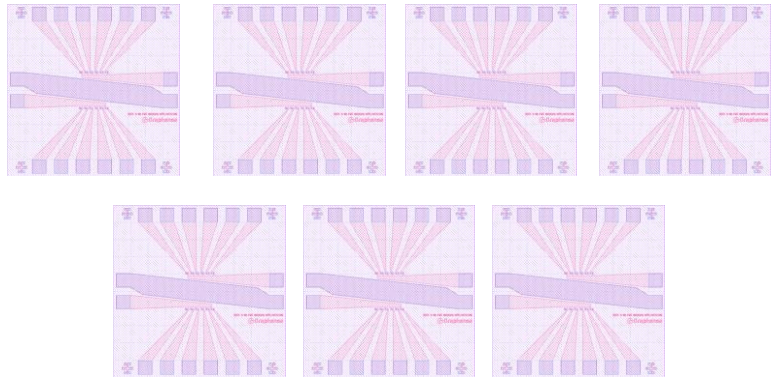


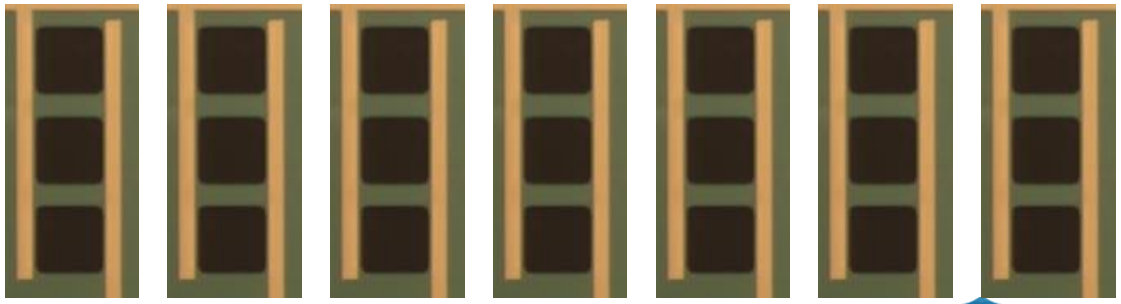
(0.9)^7≈0.49

n is number of targets,

functionalization, etc…





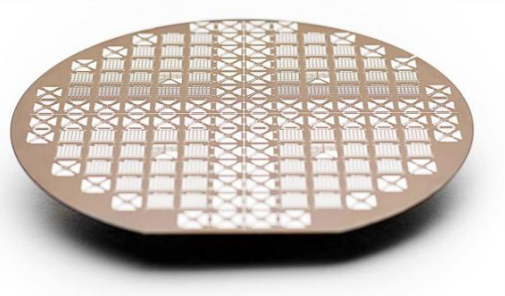


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Take away messages

- Graphene has great opportunities to revolutionize healthcare and PoC diagnostics
- The TRL/maturity is already good for such applications
- A “holistic/STCO” approach is necessary when creating biosensing devices, taking into account die, functionalization, packaging and form factor of the final products







Graphenea

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