Graphenea/AMO hands-on training

2D PILOT LINE

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the European Union

2 November 2026

Outline

- Introduction
- Graphenea's PDK
  - PDK Documents
- AMOs PDK Overview
  - Exemplary PDK of MPW run #3
  - PDK Documents (GDS template, DRC script)
- Introduction Klayout
  - Interface, Layout, Layers, Structures
- Create a simple Device (GFET)
  - Draw structures in different layers
  - Make an array of the device
  - Design Rule Check (DRC)
- Use Graphenea's or AMO's GDS file to draw your test structures

13.00 – 14.00	AMO/Graphenea hands-on session: Introduction to KLayout, PDK and DRC analysis
Coffee break (14:00 – 14:30)	
14:30 – 17:00	AMO/Graphenea hands-on session: exercises
End DAY 1	



INTERACTIVE

2D PILOT LINE

AMO

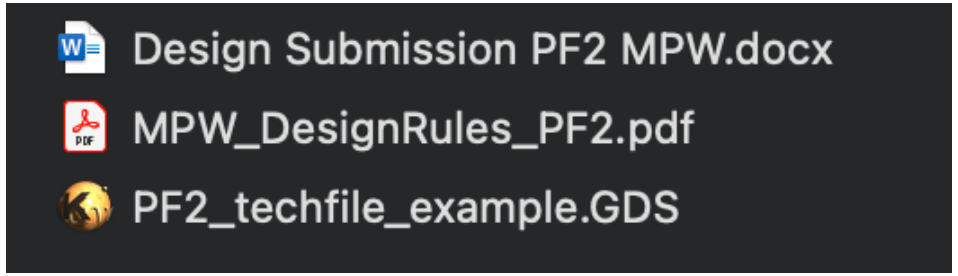
Graphenea

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Graphenea’s PDK



PDK documents



PDK documents

Graphenea

Design Submission Form PF2

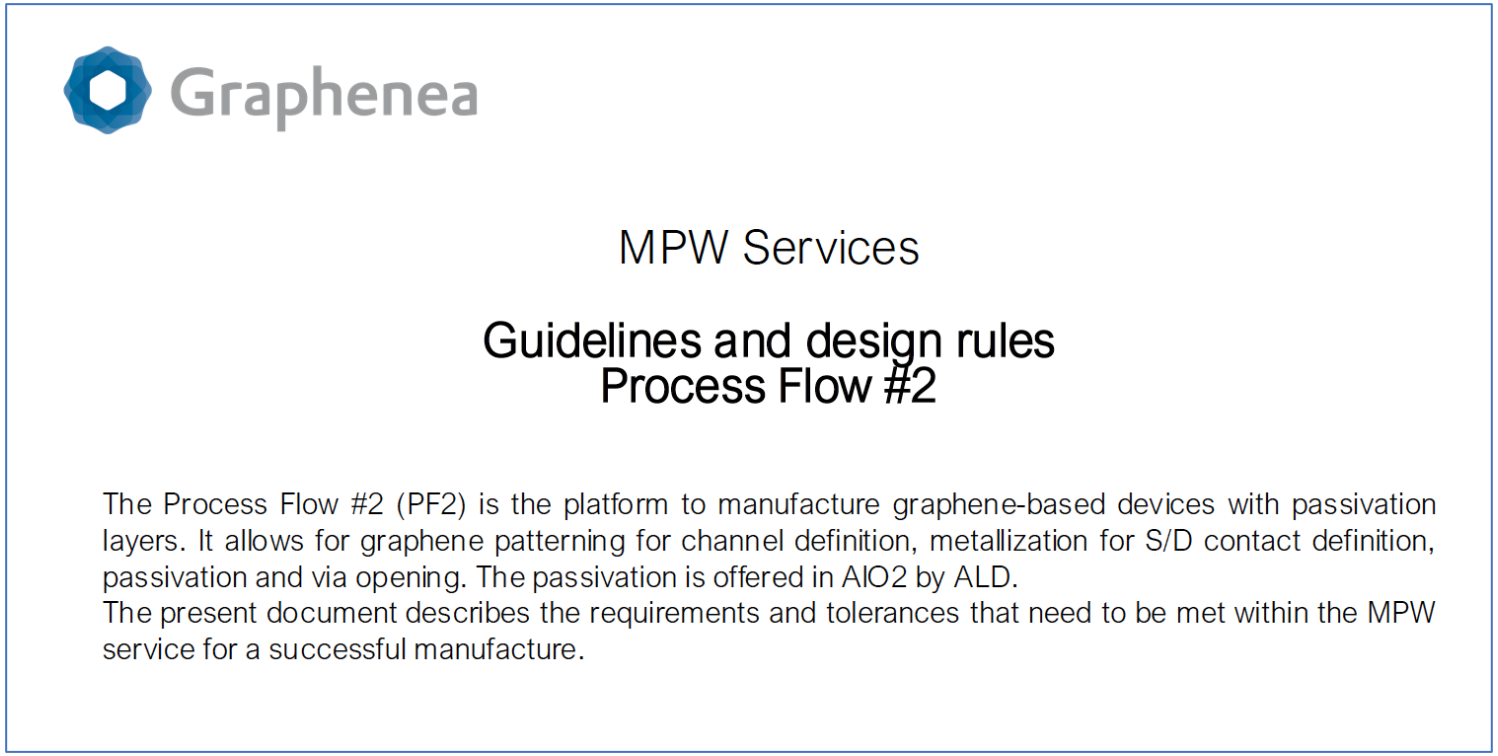
Company	
Contact name	
Contact affiliation/position	
Contact Email	

·Make sure your design is compatible with the process flow design rules to speed up the submission process.
·Data file must be in .gds format
·

File name	

PF2 layer	Data layer name	Critical Dimension
Die	0/1	-
Graphene	1/0	
Metal	2/0	
Via opening	3/0	

PDK documents – MPW guidelines and design rules



PDK documents – MPW guidelines and design rules

Process details and materials

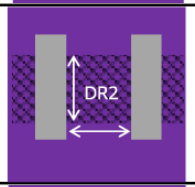
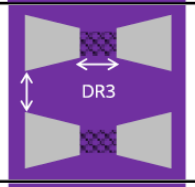
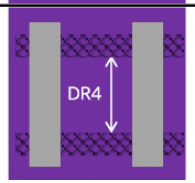
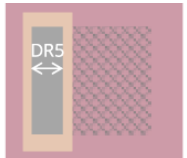
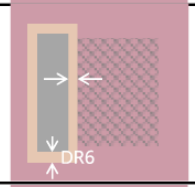
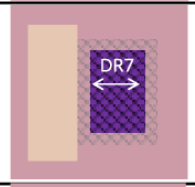
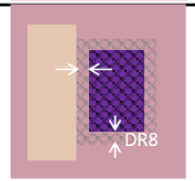
- Graphene patterning
- Graphenea's Au contacts (50 nm)
- Thickness accuracy: +/- 5 nm

ALD passivation

- Dielectric material: Al_2O_3
- Thickness: 50 nm
- Thickness accuracy: +/- 3 nm
- Via opening

➢ Compatible with both mild and strong solvents.

PDK documents – MPW guidelines and design rules

Design Rules			
DR1	Minimum feature size – metal	10 µm	
DR2	Minimum feature size – graphene	65 µm	
DR3	Minimum feature separation – metal	50 µm	
DR4	Minimum feature separation - graphene	20 µm	
DR5	Minimum via opening size – metal	25 µm	
DR6	Minimum via opening to metal edge distance	10 µm	
DR7	Minimum via opening size – Graphene	25 µm	
DR8	Minimum via opening to graphene edge distance	10 µm	

PDK documents – MPW guidelines and design rules

Quality control

AFM roughness

- RMS roughness < 1.5 nm
- Ra roughness < 1.0 nm

Raman

- I(G)/I(2D) < 1.25
- I(D)/I(G) < 0.15
- Pos(G) < 1600 cm^{-1}
- FWHM(2D) < 45 cm^{-1}

Carrier transport

- Mobility > 1000 $cm^2/V{\cdot}s$
- Dirac point < 50 V in 90 nm SiO_2 backgate
- Hysteresis < 20 V @ 5 V/s

We set the following thresholds to define a successful die

Optical microscopy

- Channel integrity/coverage > 95%
- Device yield within die > 75%

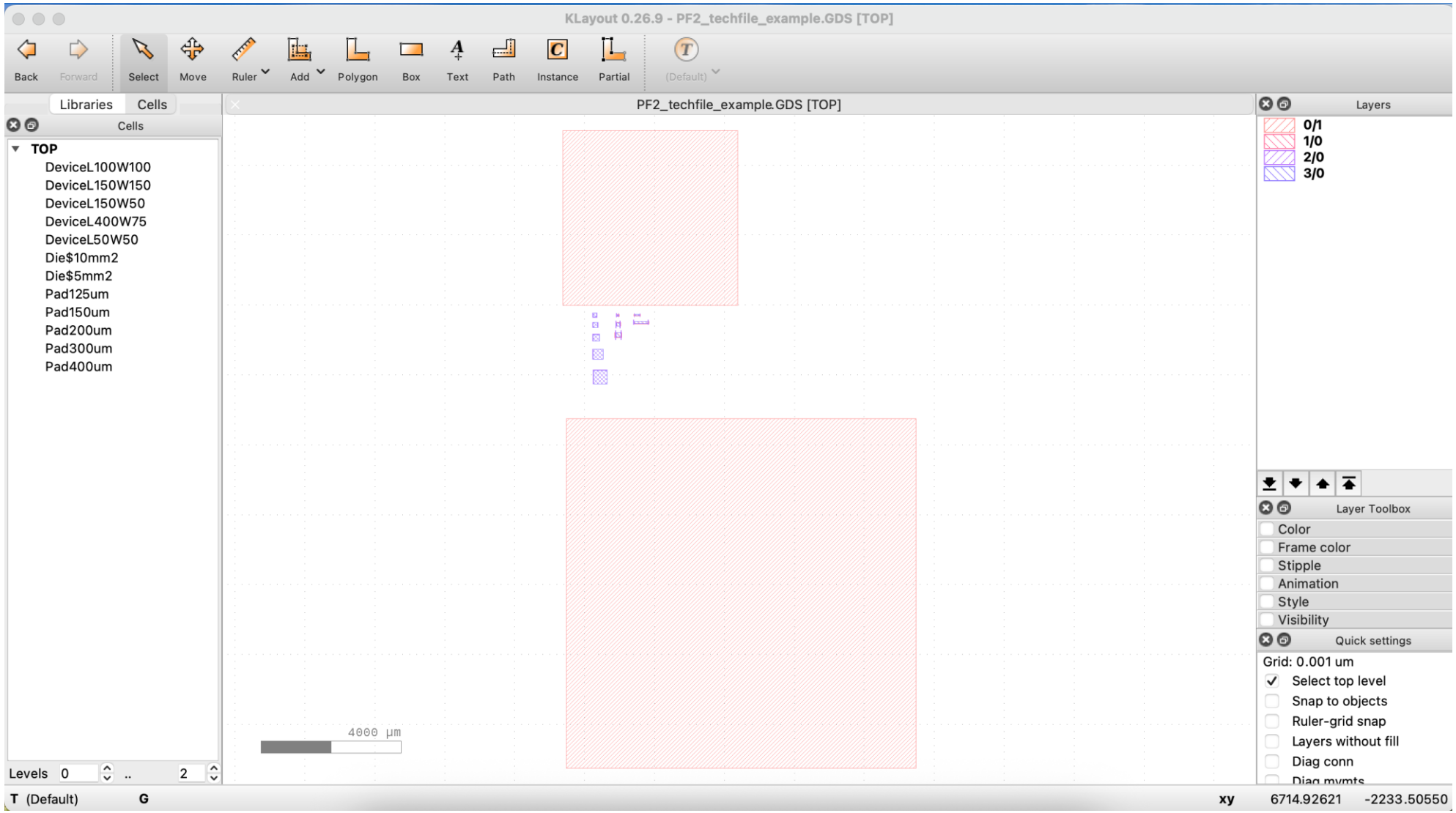
PDK documents – MPW guidelines and design rules

Aspect ratio considerations

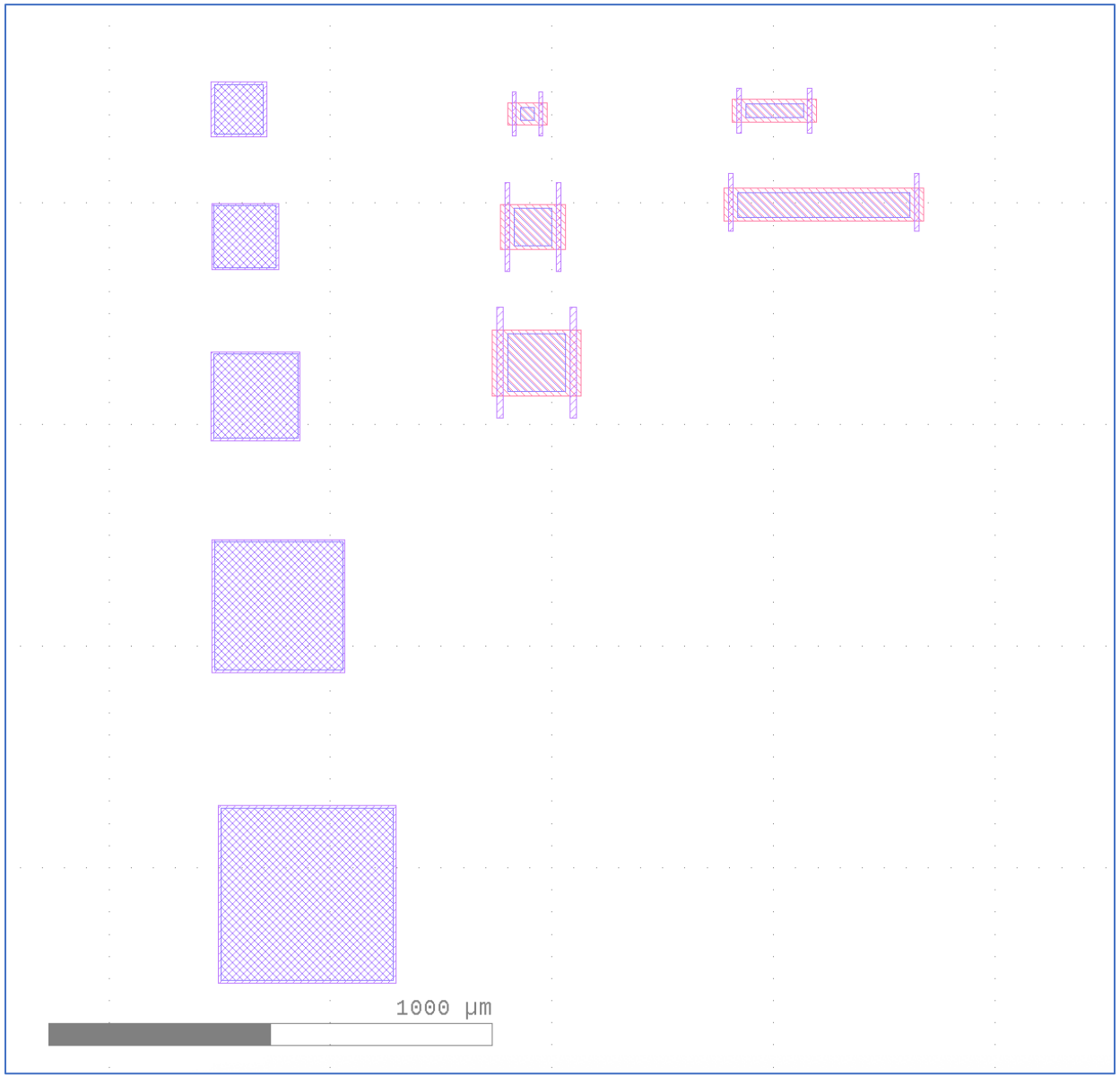
We strongly recommend you to adhere to the aspect ratio guidelines to enhance or worsen the mobility of your device. Deviations from these aspect ratios can result in anomalous mobilities.

Device width (µm)	L/W
<20 µm	>4
20-50	>2
>100	>1

PDK documents – Klayout techfile



PDK documents – Klayout techfile



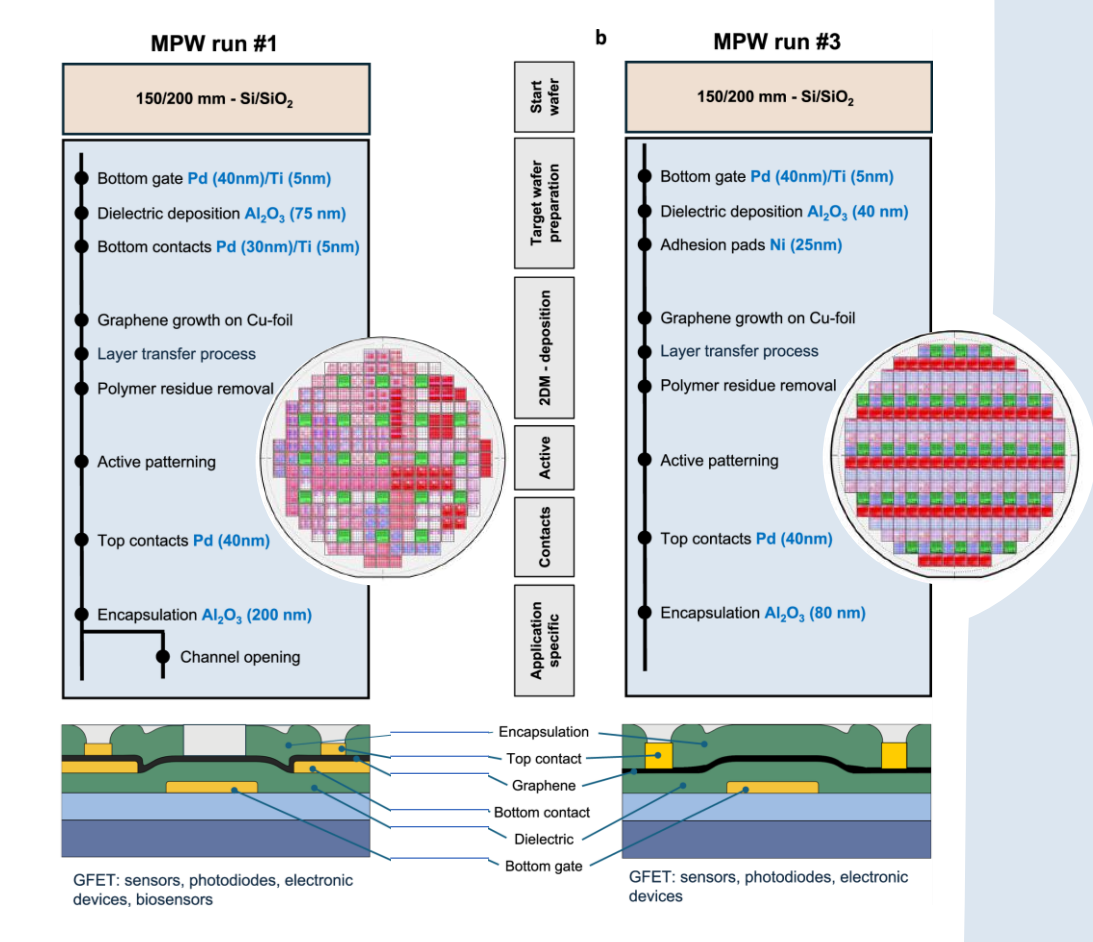
Graphenea

AMO PDK Training

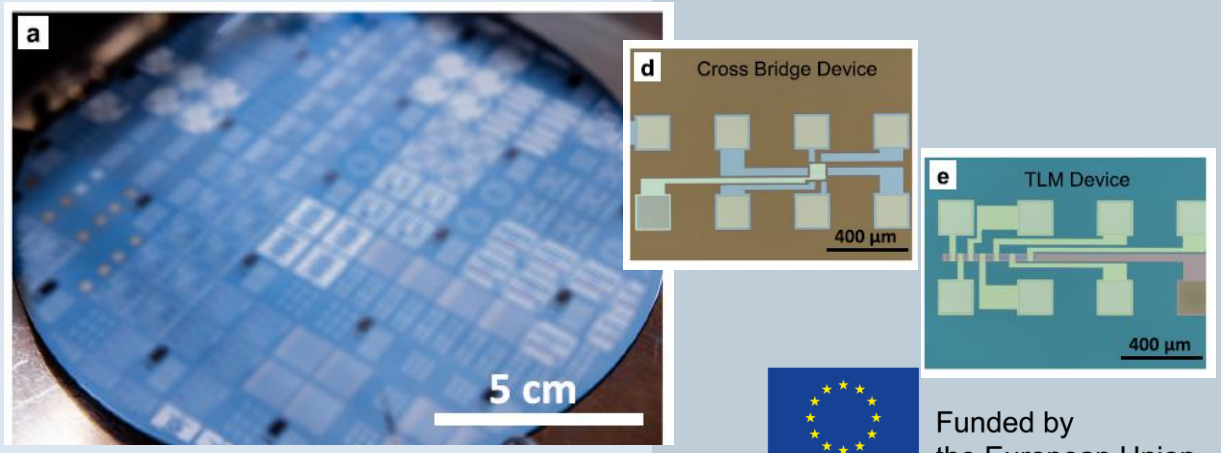
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Wafer-scale Graphene MPW Runs @ AMO



- Two MPW runs attracted **60 applications** and produced orders from **19 entities**.
- **MPW run 1** was intended mainly for graphene-based sensors
  - Sandwich contact
  - Encapsulation: 200 nm evaporated Al2O3
- **MPW run 3** focused on graphene electronics
  - Top contact
  - Encapsulation: 80 nm ALD Al2O3

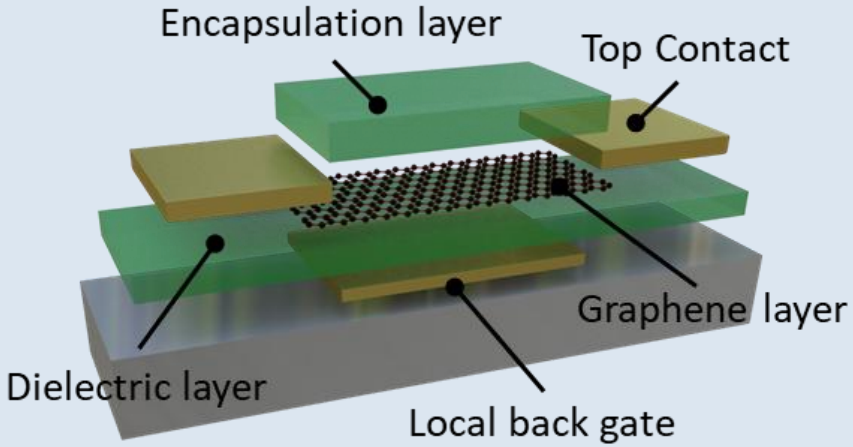


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Canto *et al.* . *Nat Commun* **16**, 1417 (2025). https://doi.org/10.1038/s41467-025-56357-0

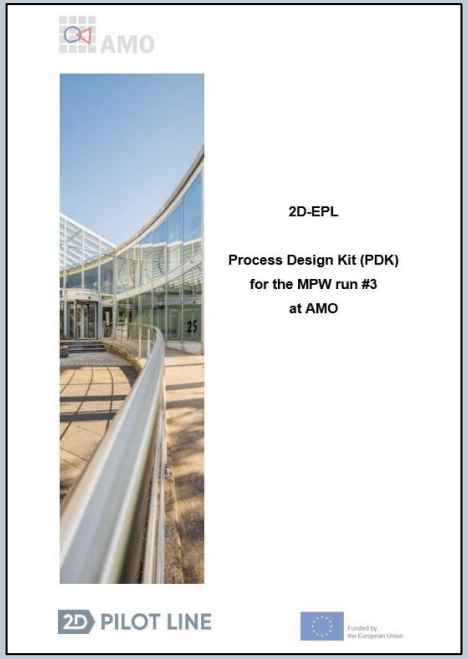
PDK for the Multi-Project-Wafer Run #3 at AMO

- The offered device structure is an encapsulated GFET with top contacts and local back gate.
- 6 Layers
- The design of the device can be adjusted within the specifications.



Layer Thicknesses

	Rigid Substrate	Si/SiO_2	90 nm
1	Back Gate Contact	Ti/Pd	5nm /40nm
2	Dielectric Layer	Al_2O_3	40 nm
3	Adhesion Layer for Top Contact Pad	Ni	25 nm
4	Graphene	Single layer, CVD on Cu	
5	Top Contact	Pd	40 nm
6	Encapsulation	Al_2O_3	80 nm



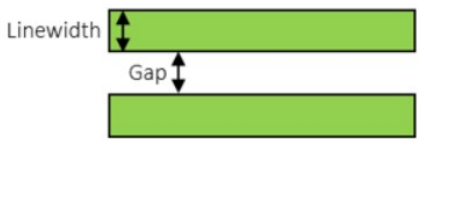
Details in PDK documents explained

2D PILOT LINE

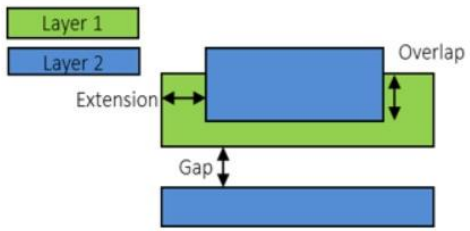
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Design Rule

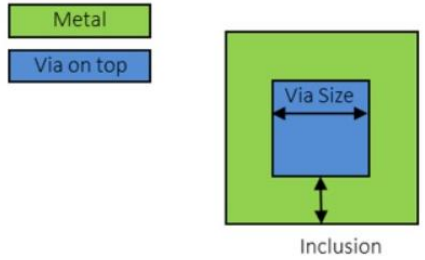
- The critical dimensions (CDs) are the physical limits of the process.
- **The general design rule is 10 µm** for in-layer critical dimension and over-layer alignment.
- Design Rule Check (DRC) is provided with GDS file



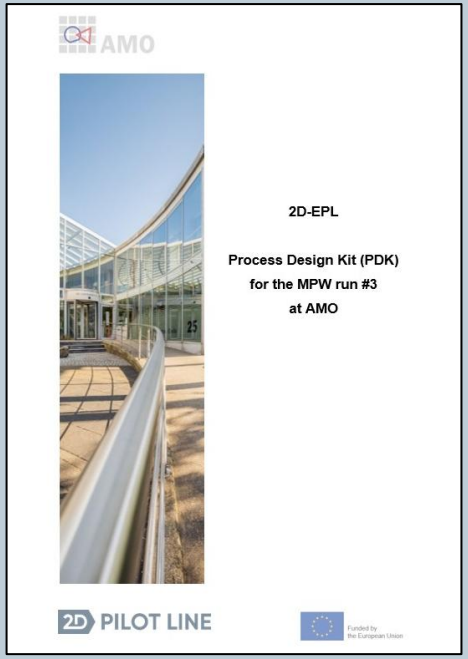
Intra-layer design	
Linewidth	≥ 10 µm
Gap	≥ 10 µm



Over-layer tolerance	
Gap	≥ 10 µm
Overlap	≥ 10 µm
Extension	≥ 10 µm

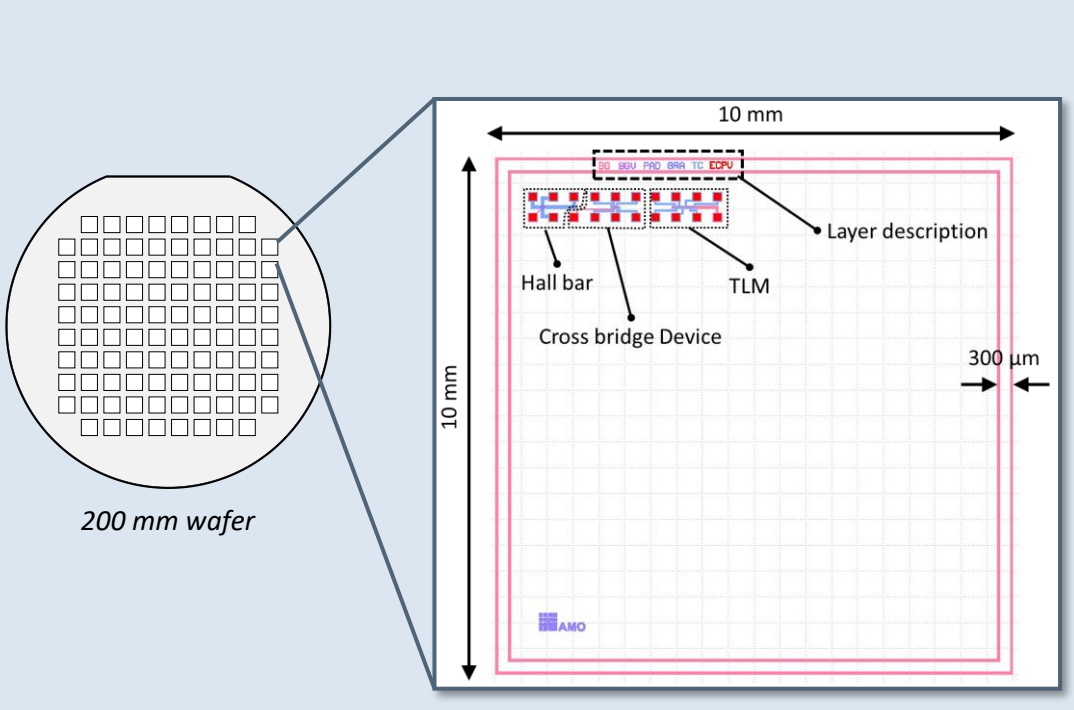


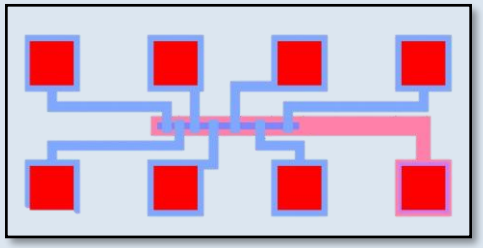
Minimum via dimensions	
Via Size	≥ 10 µm
Inclusion	≥ 10 µm

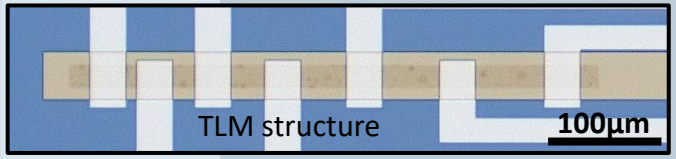


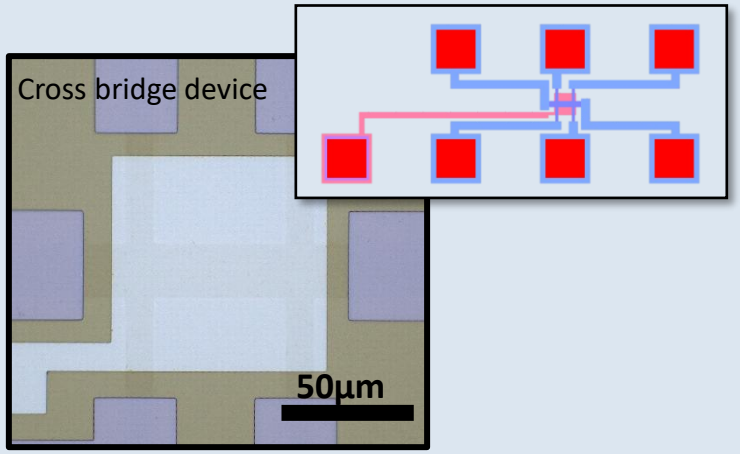
Details in PDK documents explained

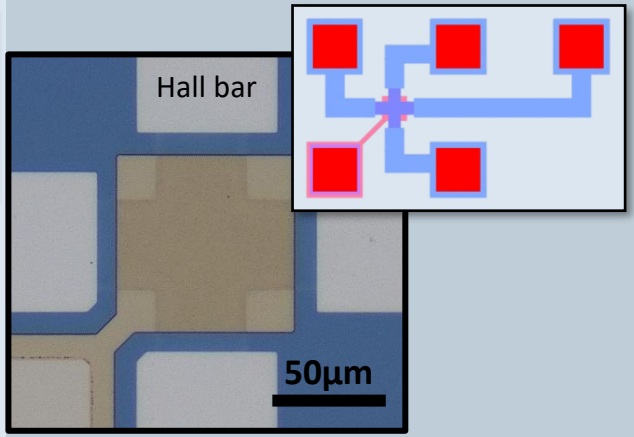
Die Design and Device Library











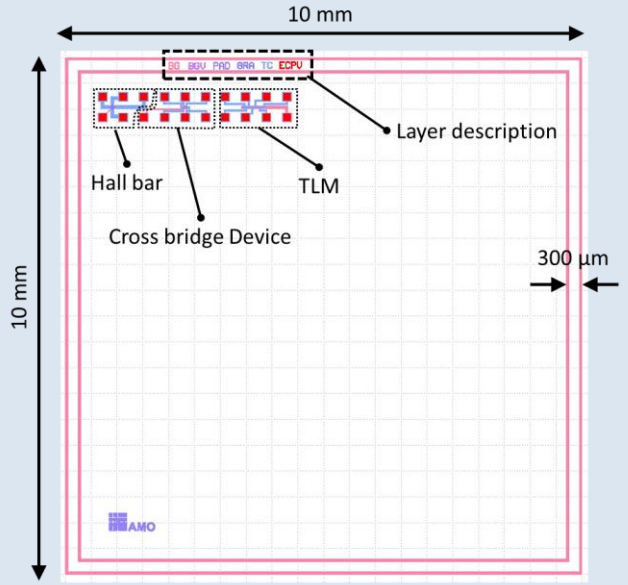
- The design of the dies with the size of 10 mm x 10 mm can be individually within the design rules.
- Device Library available for reference devices available (hall bar, four-point, TLM device) as a basis for further modifications
- Details in PDK and GDS template file

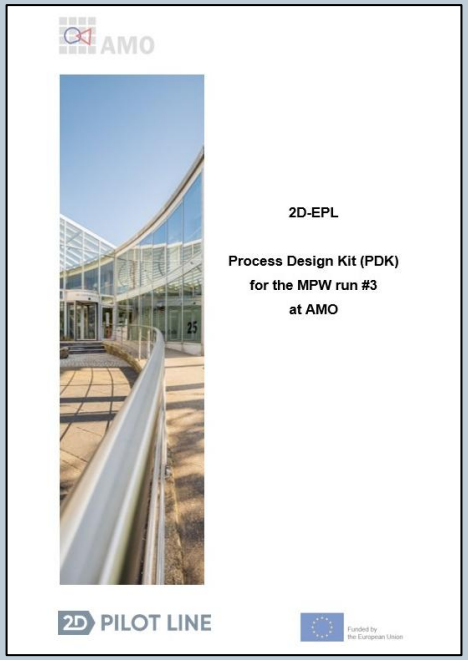
2D PILOT LINE

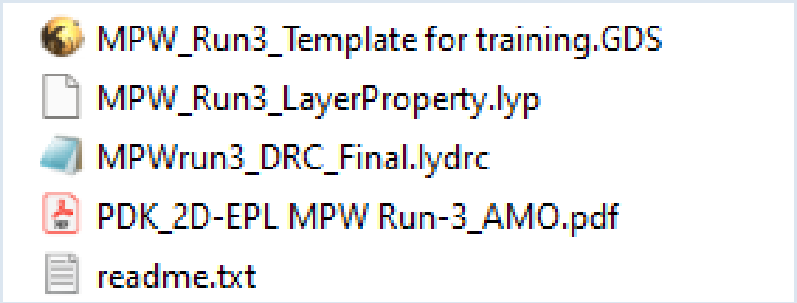
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Provided Files

- GDS template file
- Layer Name file
- DRC code
- PDK Document
- Readme file for loading and running the DRC file





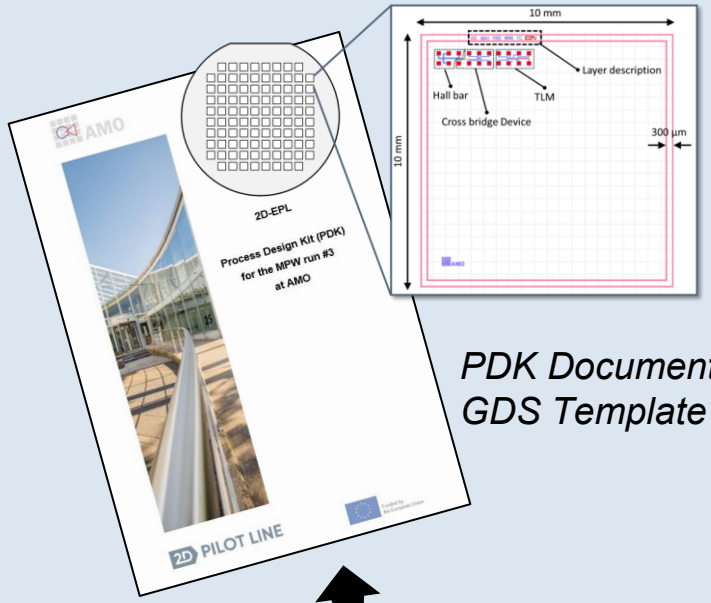


the DRC files (in phyton) have to stay in the same folder as the design

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How does it work?



PDK Document
GDS Template file







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What is KLayout?

- KLayout is an open-source layout viewer and editor for integrated circuit (IC) design.
- Supports formats like GDSII and OASIS.
- Offers Python and Ruby scripting for automation and customization.
- Useful for visual inspection, DRC, and layout editing.

💡 Why Use KLayout?

- Free and lightweight alternative to commercial tools.
- Highly customizable with macros, plugins, and scripts.
- Ideal for research, academia, and prototyping.
- Cross-platform: Windows, Linux, macOS.

```
# The PCell declaration for the circle
class StarPCell < PCellDeclarationHelper

  include RBA

  def initialize

    # Important: initialize the super class
    super

    # declare the parameters
    param(:l, TypeLayer, "Layer", :default => LayerInfo::new(1, 0))
    param(:r1, TypeDouble, "Inner radius", :default => 1, :unit => "µm")
    param(:r2, TypeDouble, "Outer radius", :default => 5, :unit => "µm")
    param(:n, TypeInt, "Number of rays", :default => 32)
    param(:da, TypeInt, "Ray angle", :default => 5, :unit => "deg")

  end

  def display_text_impl
    # Provide a descriptive text for the cell
    "StarPCell(l=#{l.to_s},R1=#{'%.3f' % r1.to_f},R2=#{'%.3f' % r2.to_f},N=#{n},da=#{da})"
  end

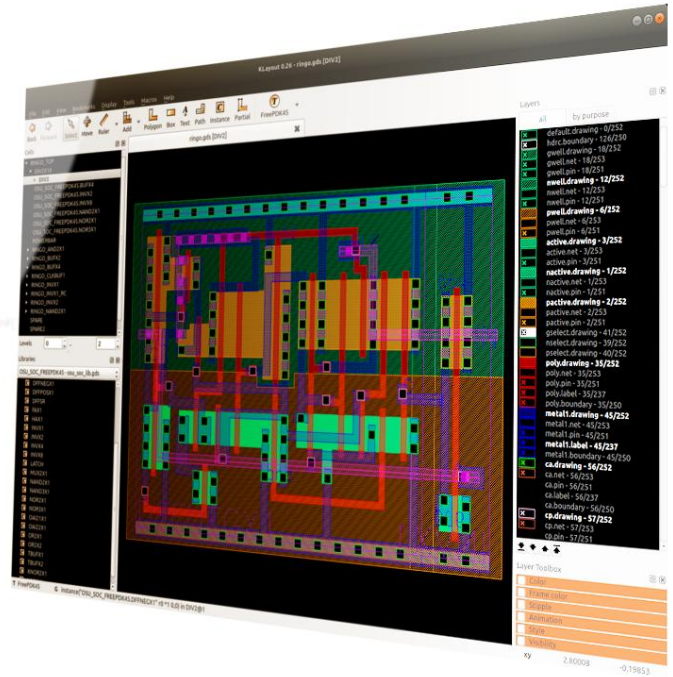
  def produce_impl

    # This is the main part of the implementation: create the layout

    # compute the ray parts and produce the polygons
    d = Math::PI * da * 0.5 / 180.0
    a = 0.0
    n.times do |i|
      dpts = [
        DPoint::new(r1 * Math.cos(a - d), r1 * Math.sin(a - d)),
        DPoint::new(r1 * Math.cos(a + d), r1 * Math.sin(a + d)),
        DPoint::new(r2 * Math.cos(a + d), r2 * Math.sin(a + d)),
        DPoint::new(r2 * Math.cos(a - d), r2 * Math.sin(a - d))
      ]
      cell.shapes(l_layer).insert(DPolygon.new(dpts))
      a += Math::PI * 2 / n
    end

  end

end
```

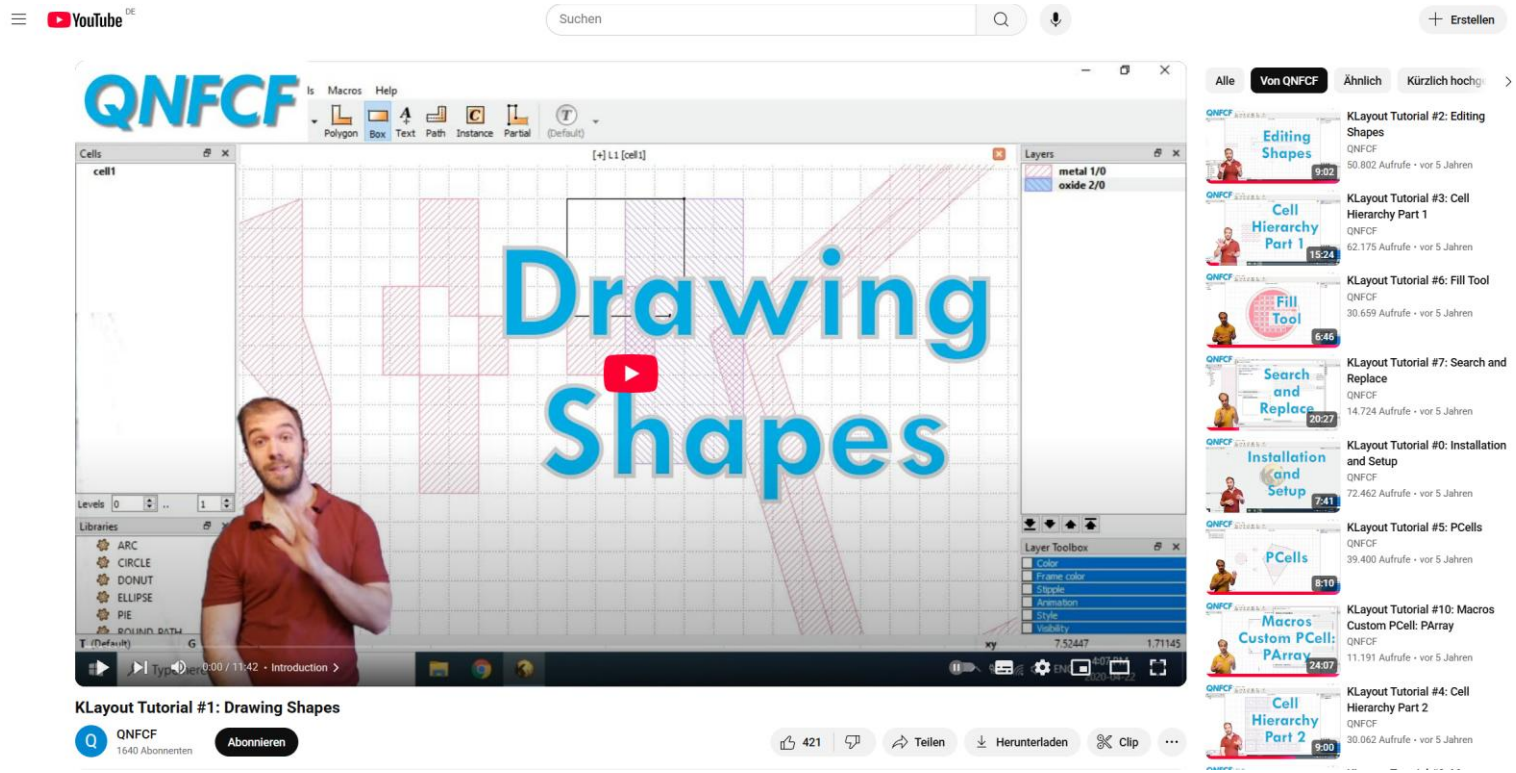


https://www.klayout.de/

Klayout Tutortials Online

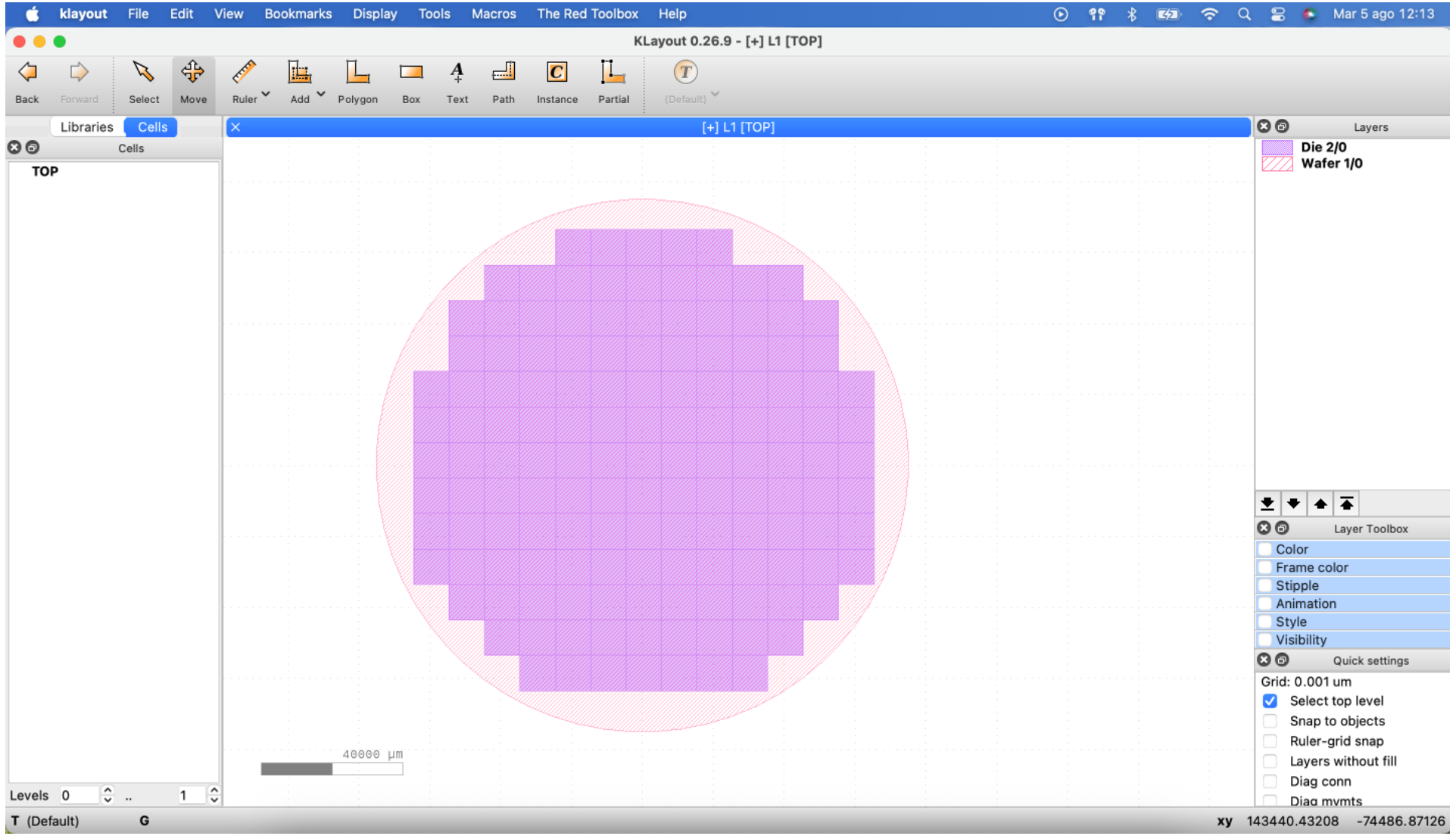
- Many Klayout Video Tutorials available

⇒ for more information or details recommended



[KLayout Tutorial #1: Drawing Shapes - YouTube]

Klayout interface



COFFEE BREAK ?!

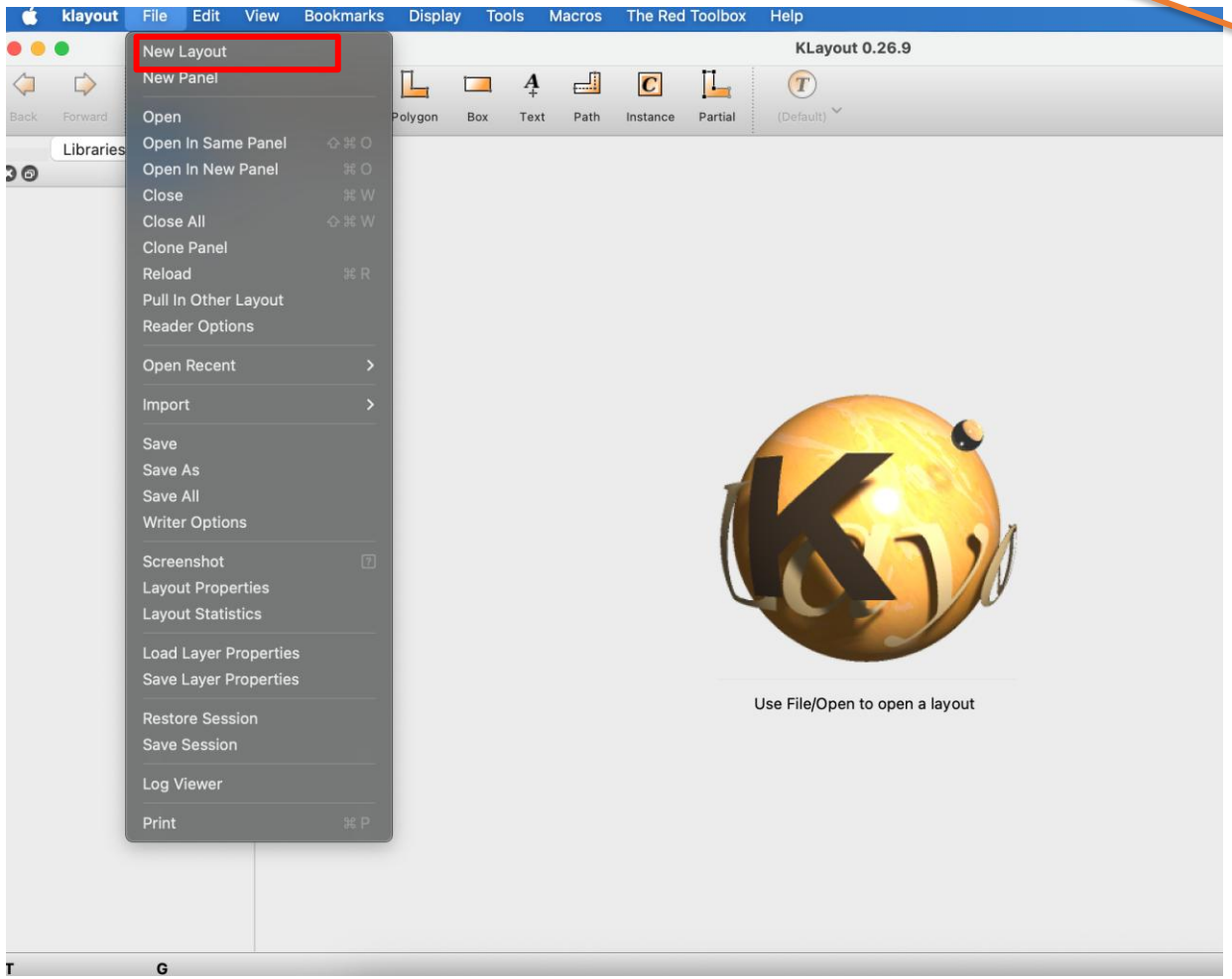
2D PILOT LINE

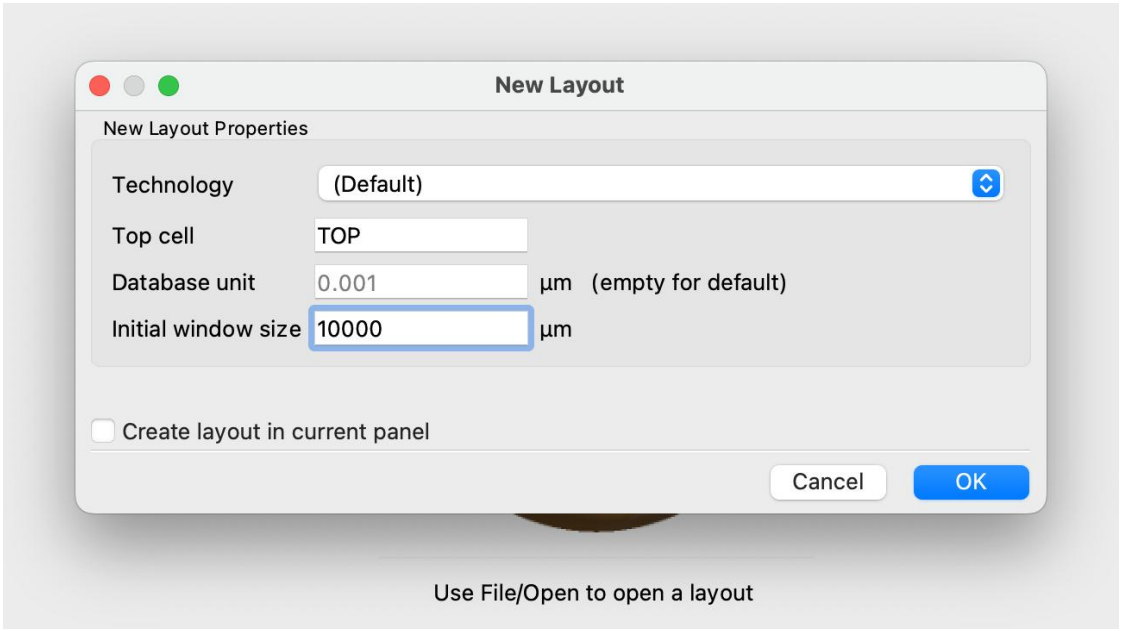
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Start a new Layout

File / New Layout → New window will open

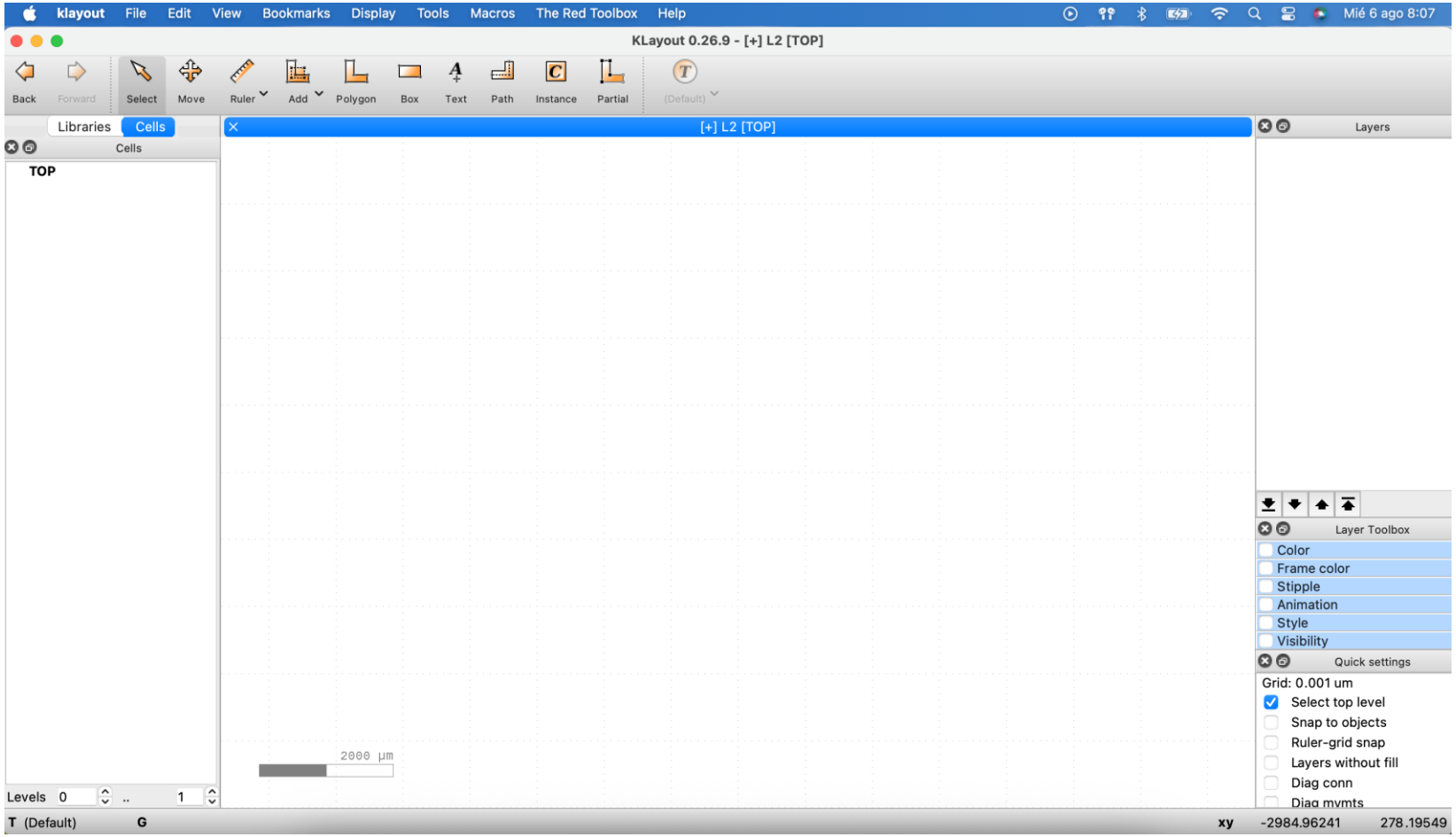




We can name the Top Cell and select the size of our initial working window

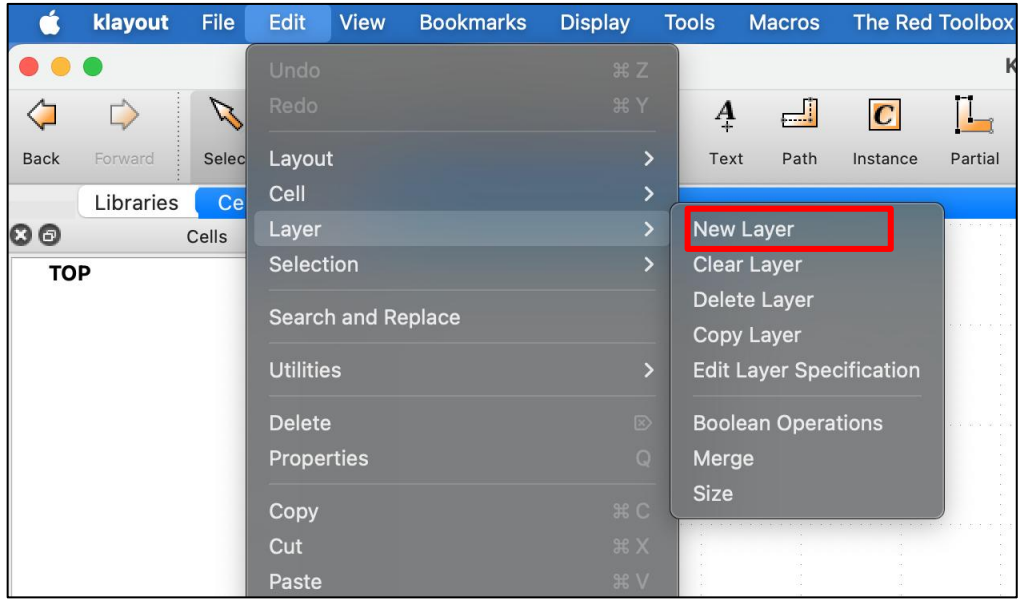
Layout window

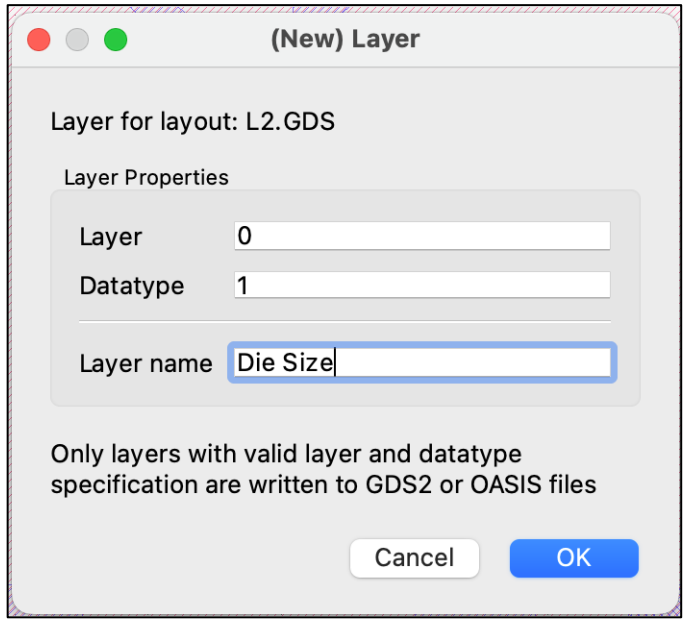
Layout window

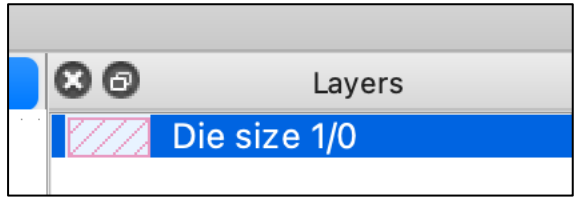


New layers

Edit / Layer / New layer

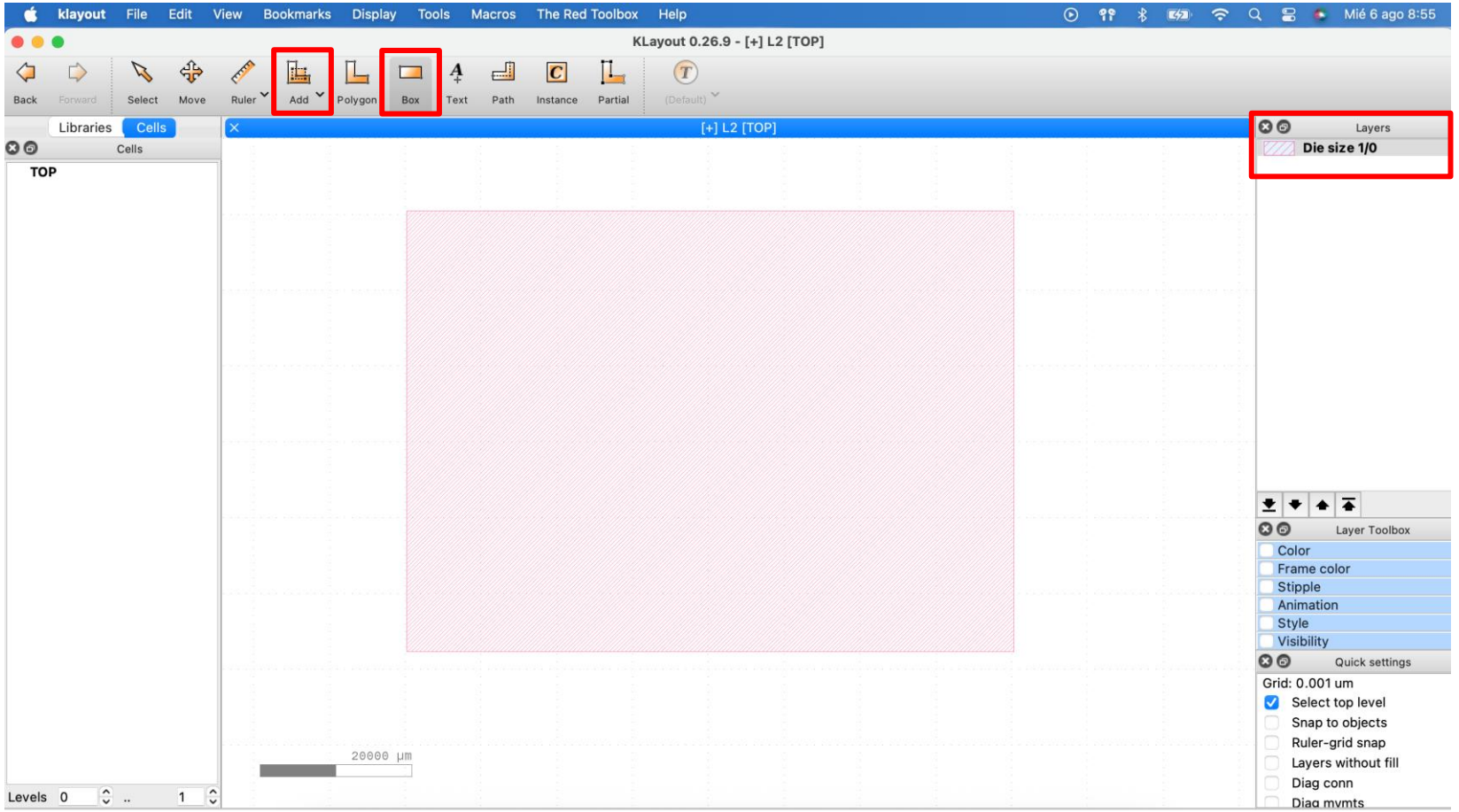






Insert structures, example: Die size

Select Layer → Add + Box



Structures sizes and position

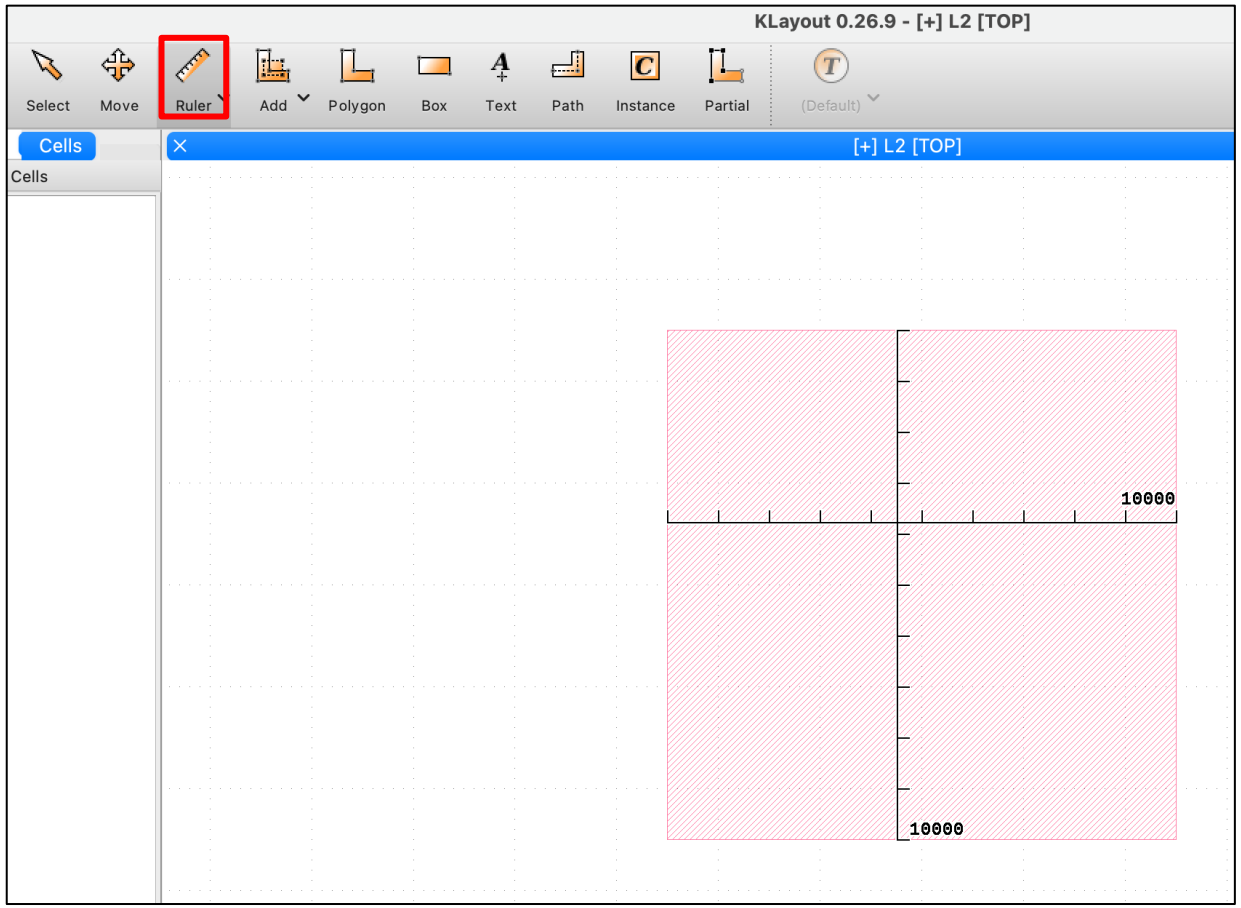
By double-clicking on the structure (or selecting the structure and pressing the 'Q' key on the keyboard)





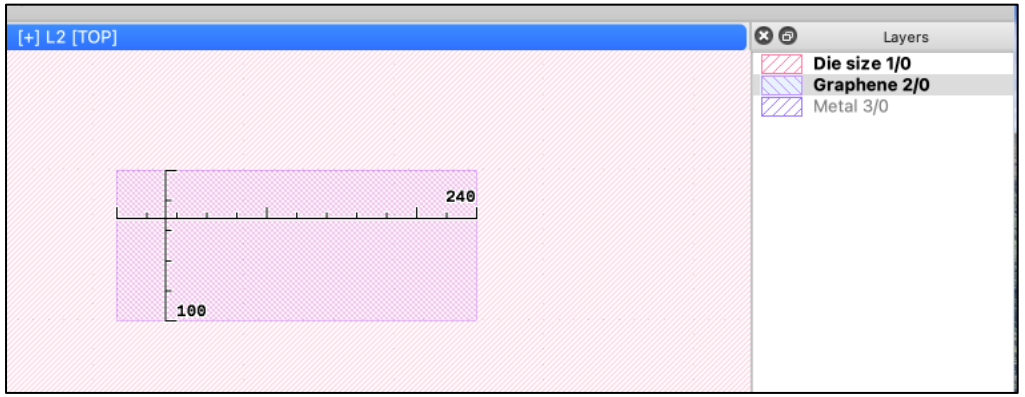
Ruler tool

Measuring structure sizes

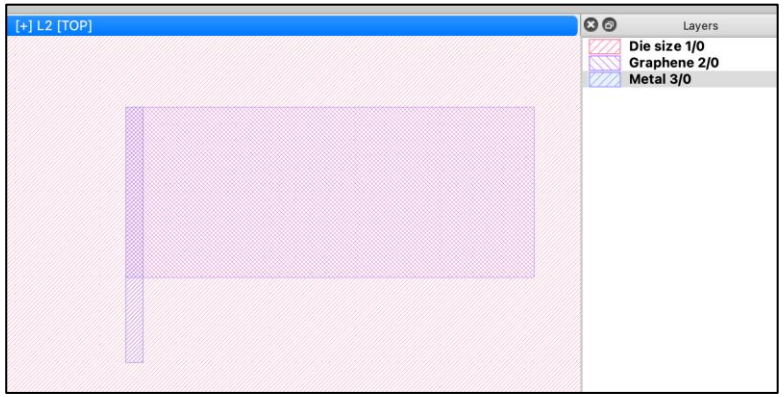


Simple device

Graphene layer

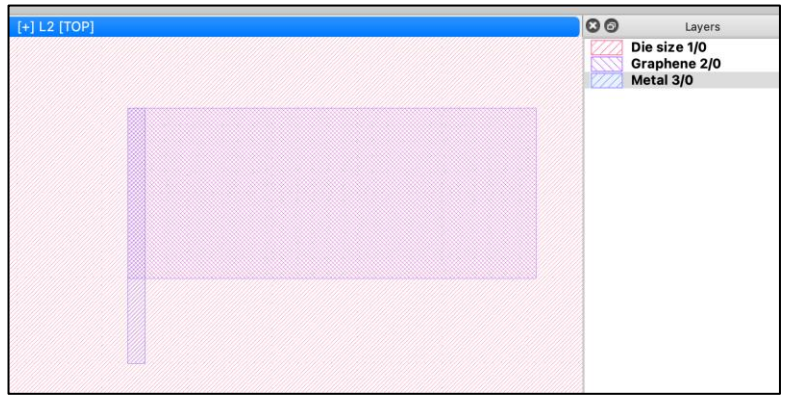


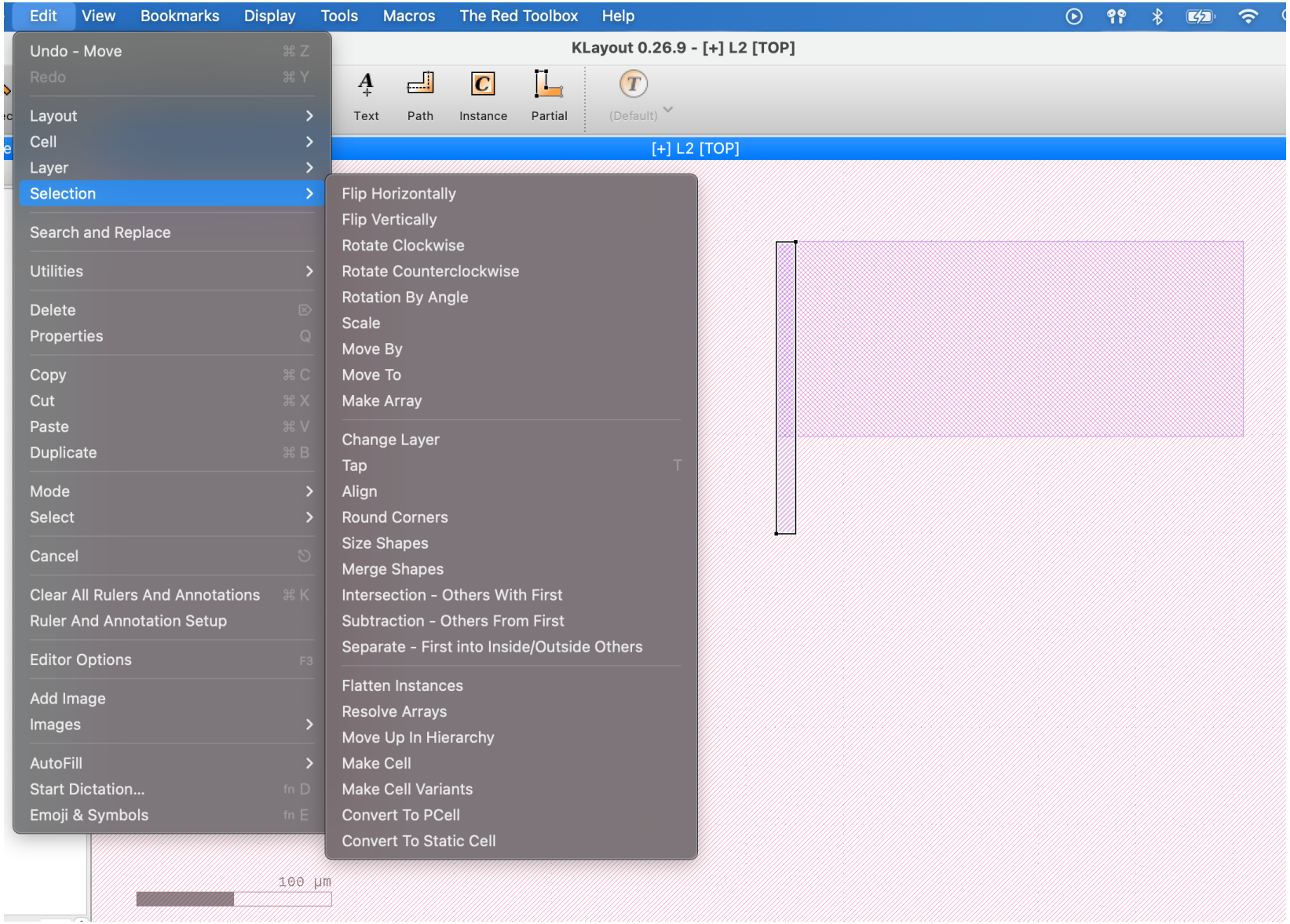
Metal layer



Simple device – Edit menu

Metal layer

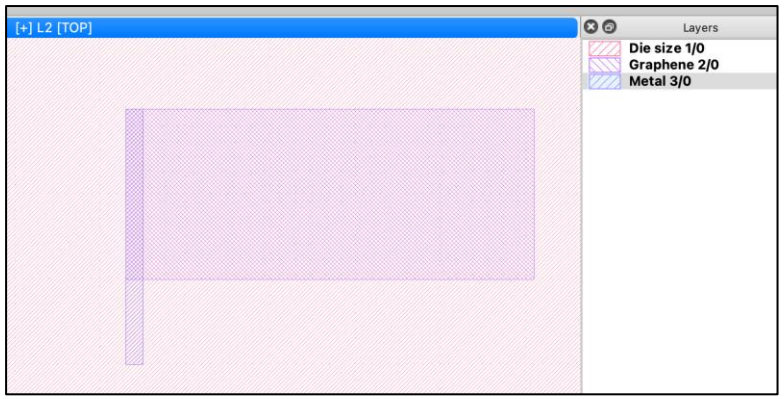


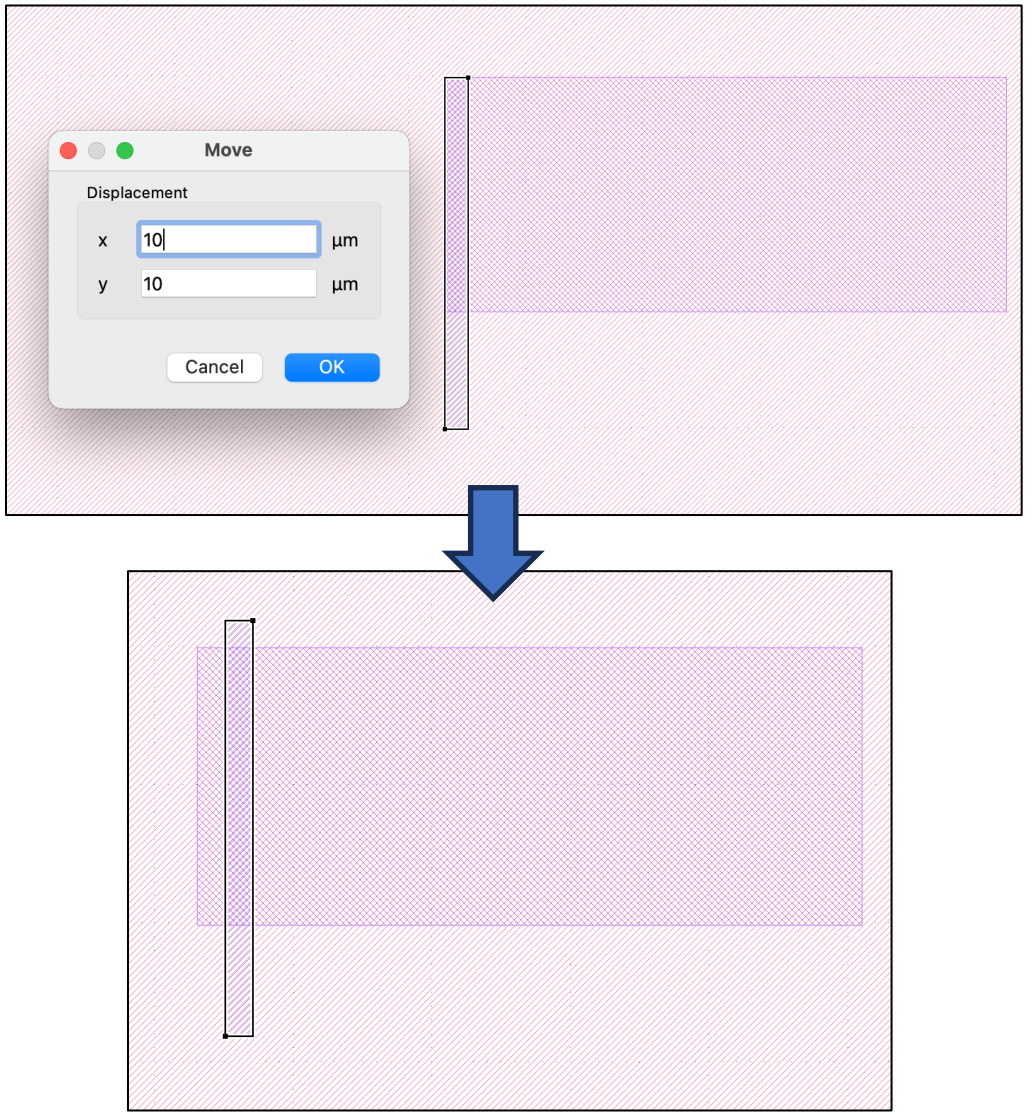


Graphenea

Simple device – Move structures

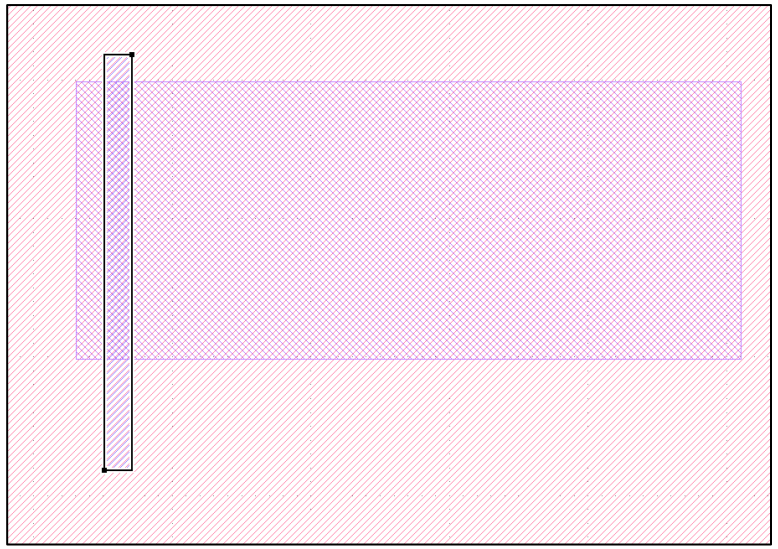
Metal layer



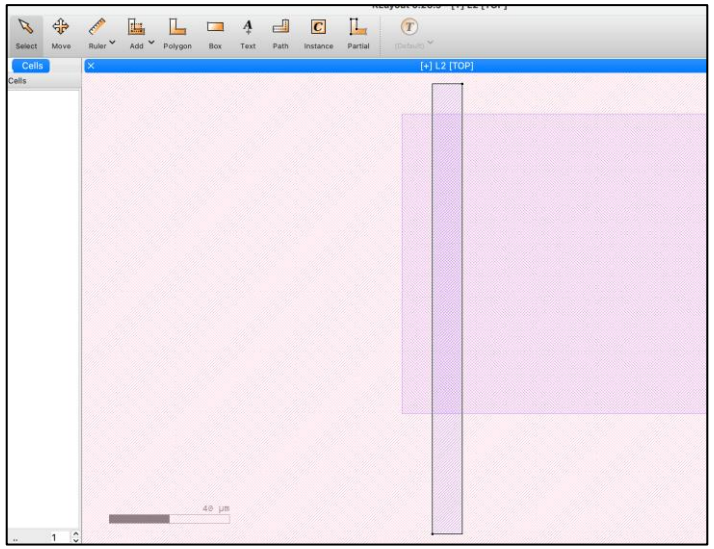


Graphenea

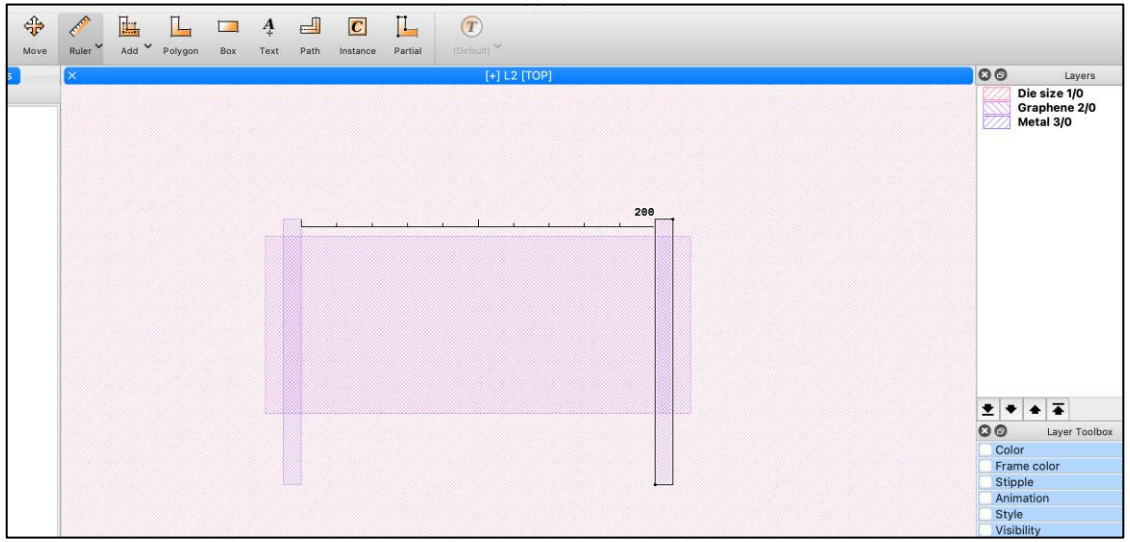
Simple device – Move structures



Select structure
+
“Ctrl” + “C”
+
”Ctrl” + “V”

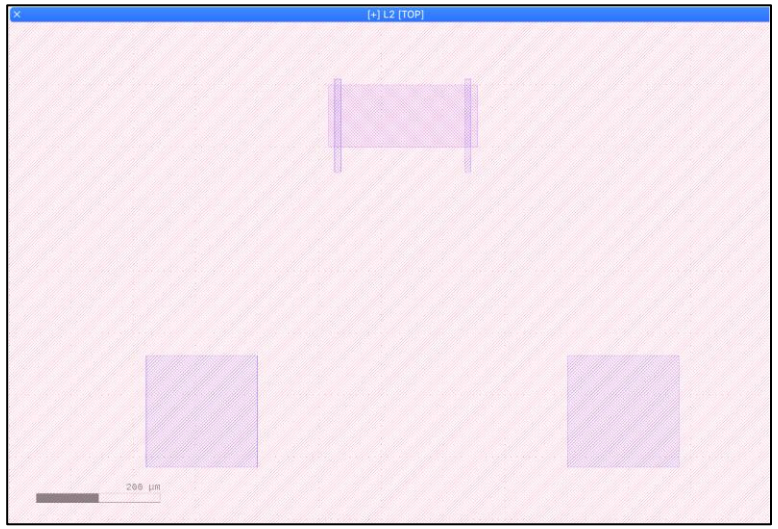


Move the new structure

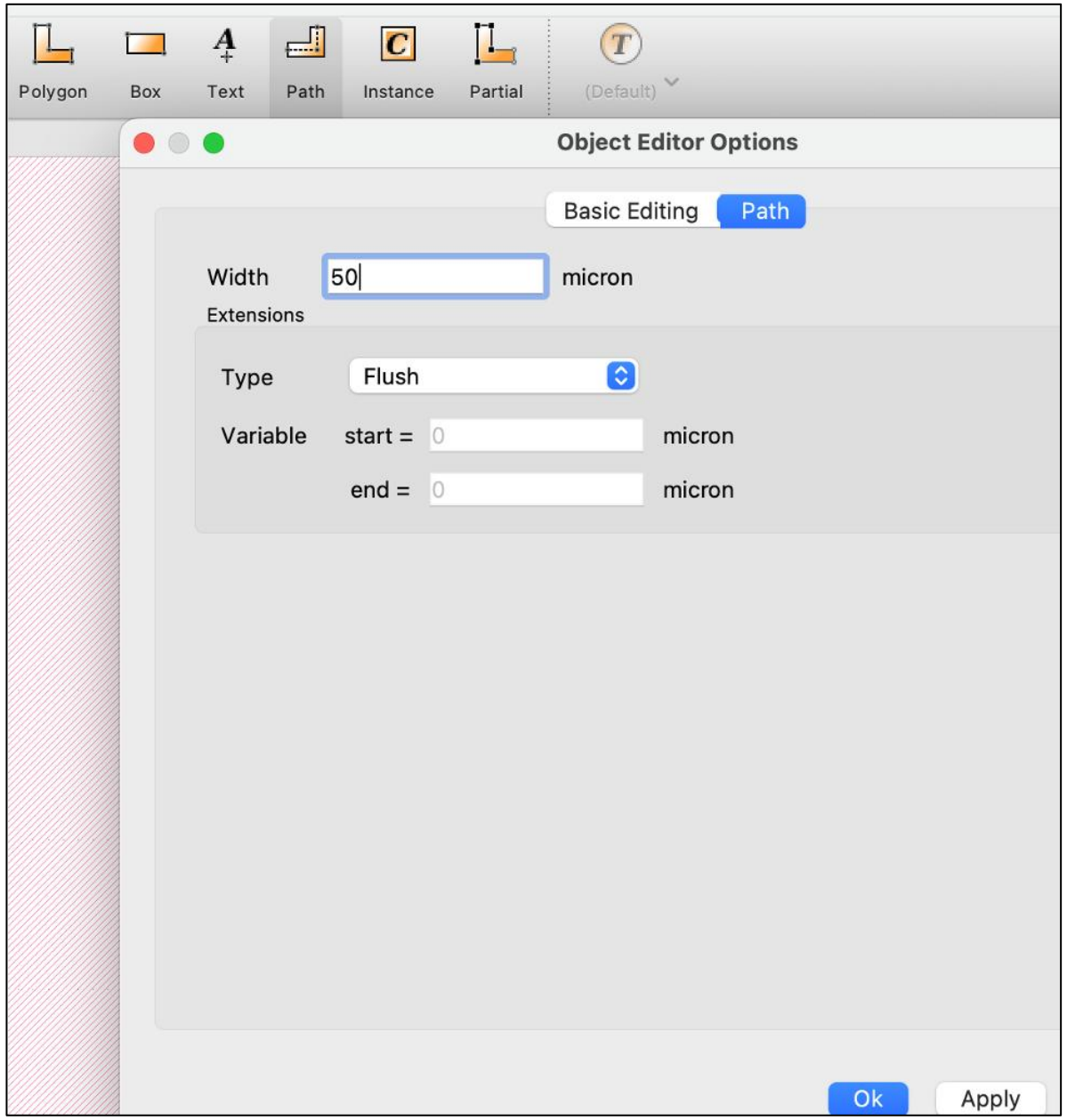


Graphenea

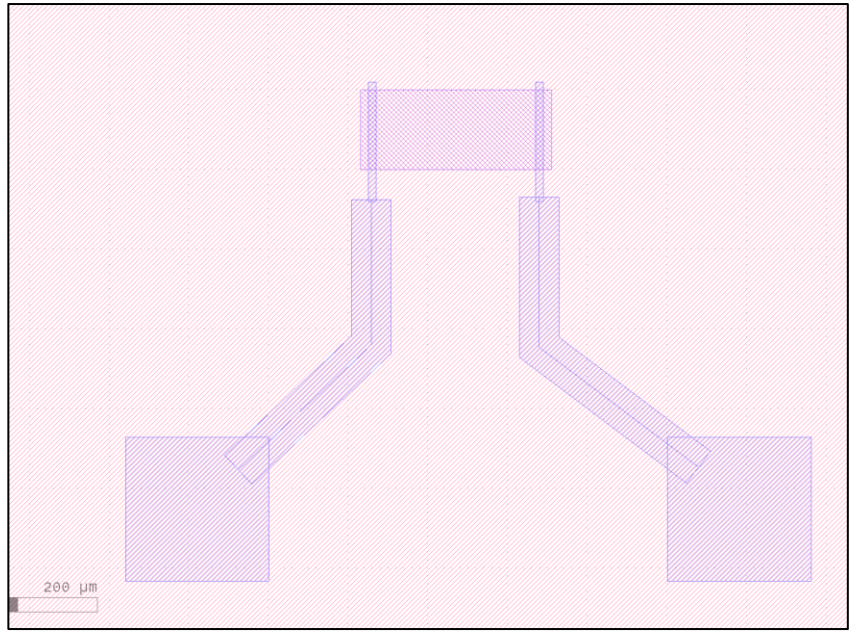
Simple device – Contacts



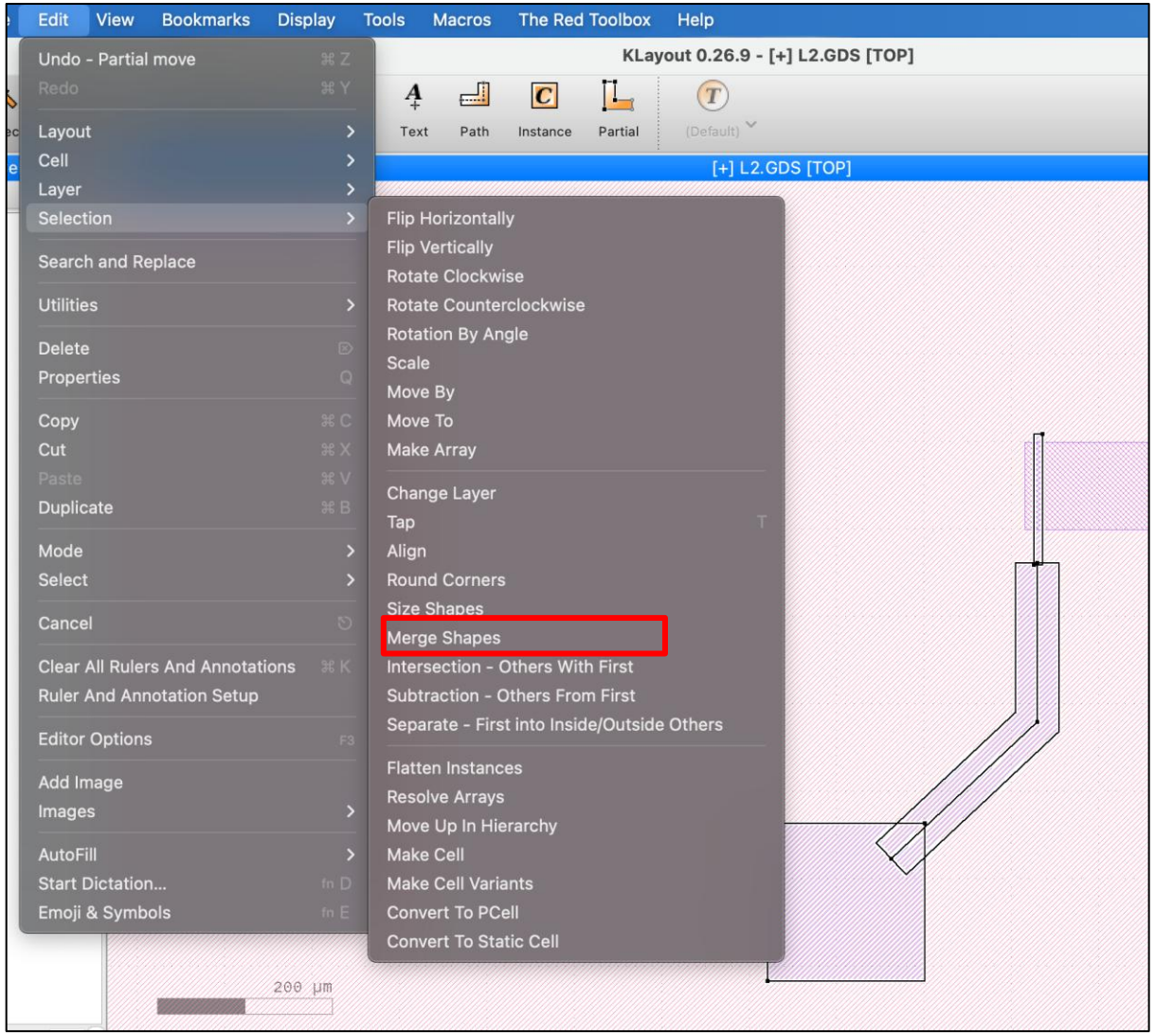
Select Metal layer
+
Tool: “Path”



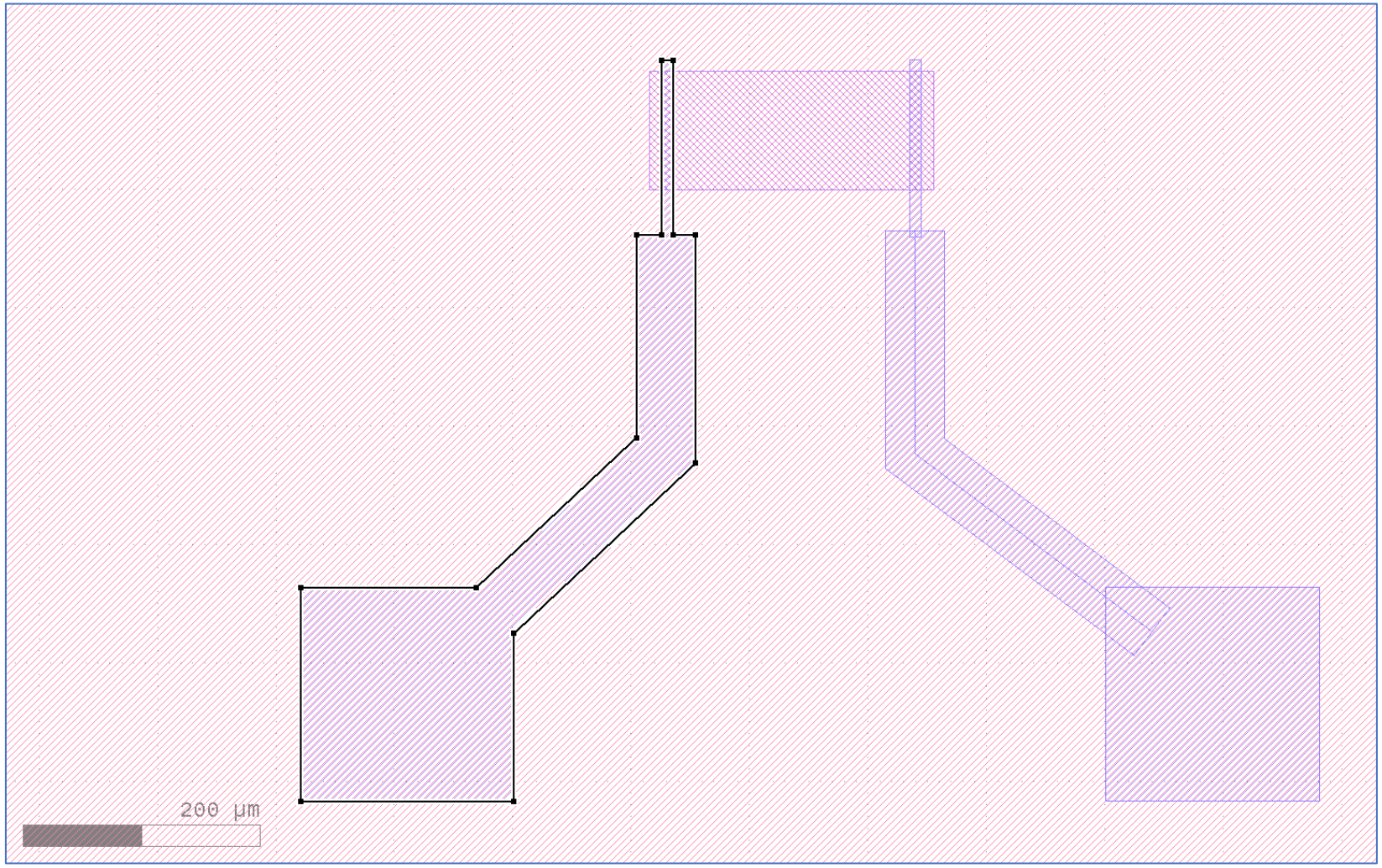
Simple device – Merge structures



“Merge” tool:
Select the structures

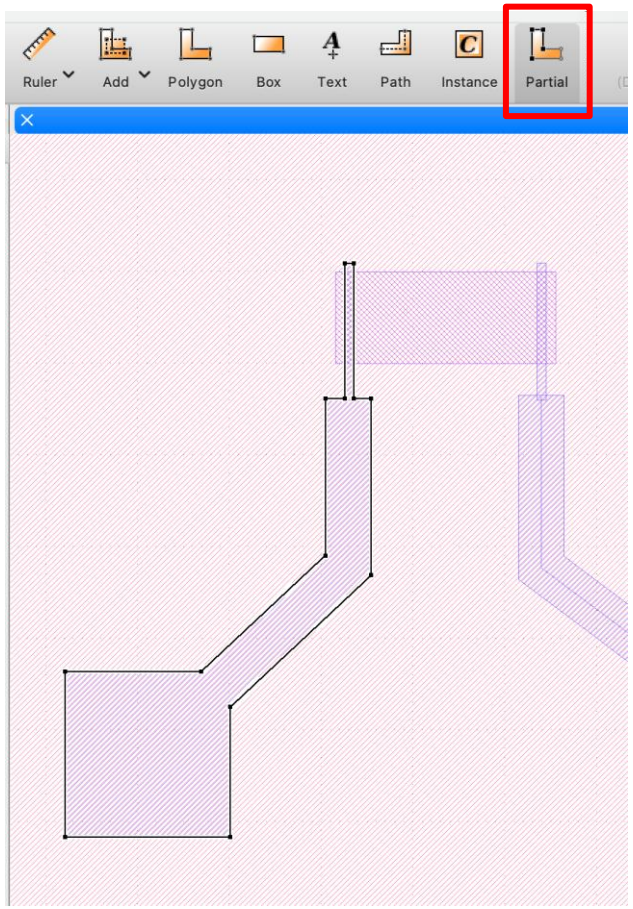


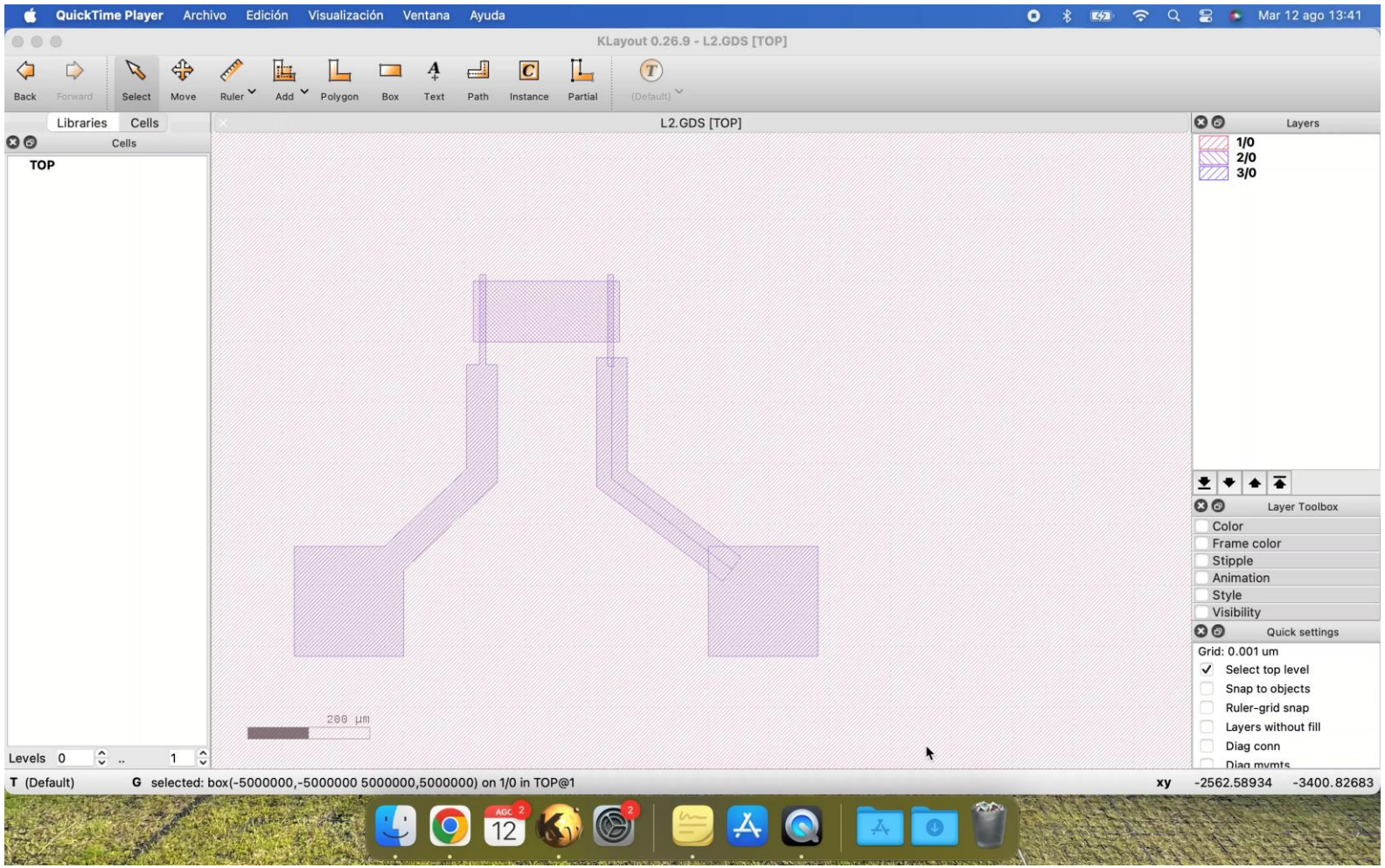
Simple device – Merge structures



Simple device – Partial tool

Select the structure
+
“Partial” tool



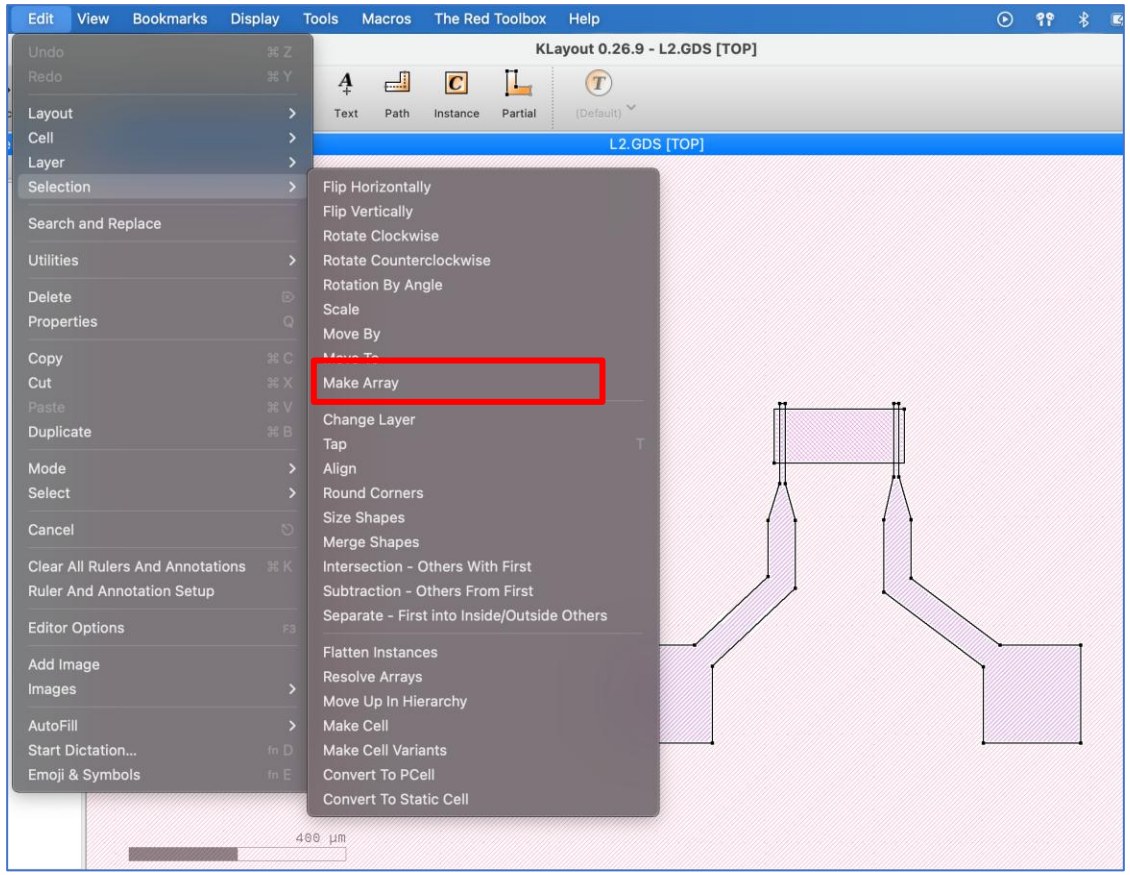


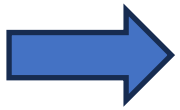
Graphenea

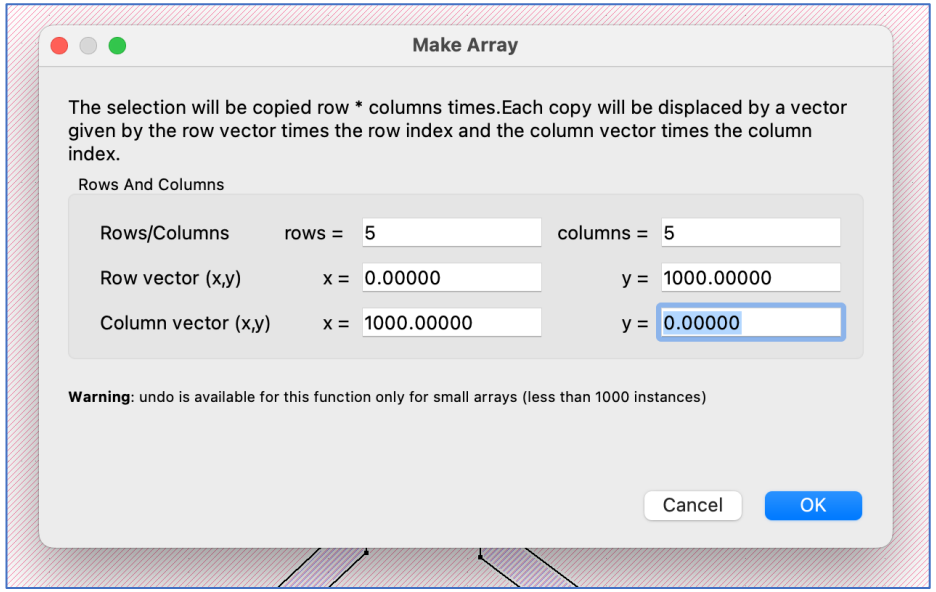
Simple device – Arrays

Option A

Select the structure + Edit + Make Array



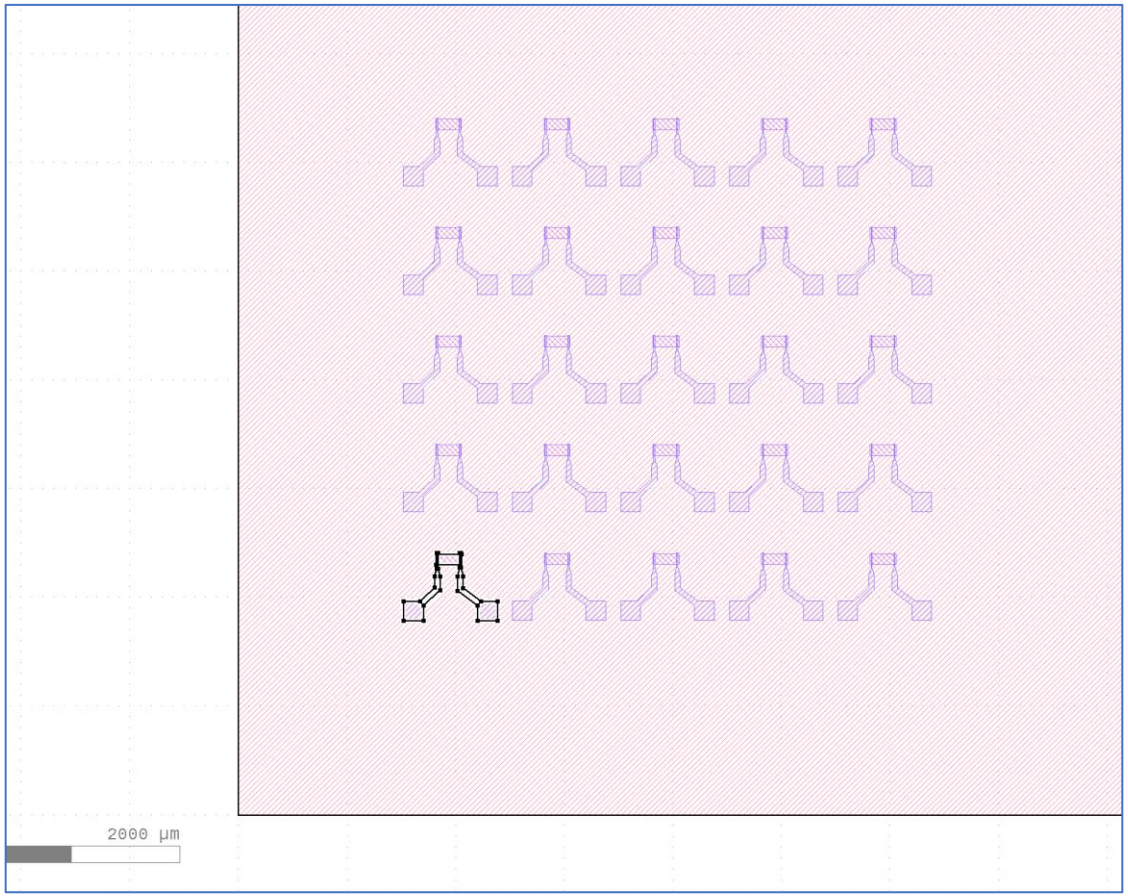




Simple device – Arrays

Option A

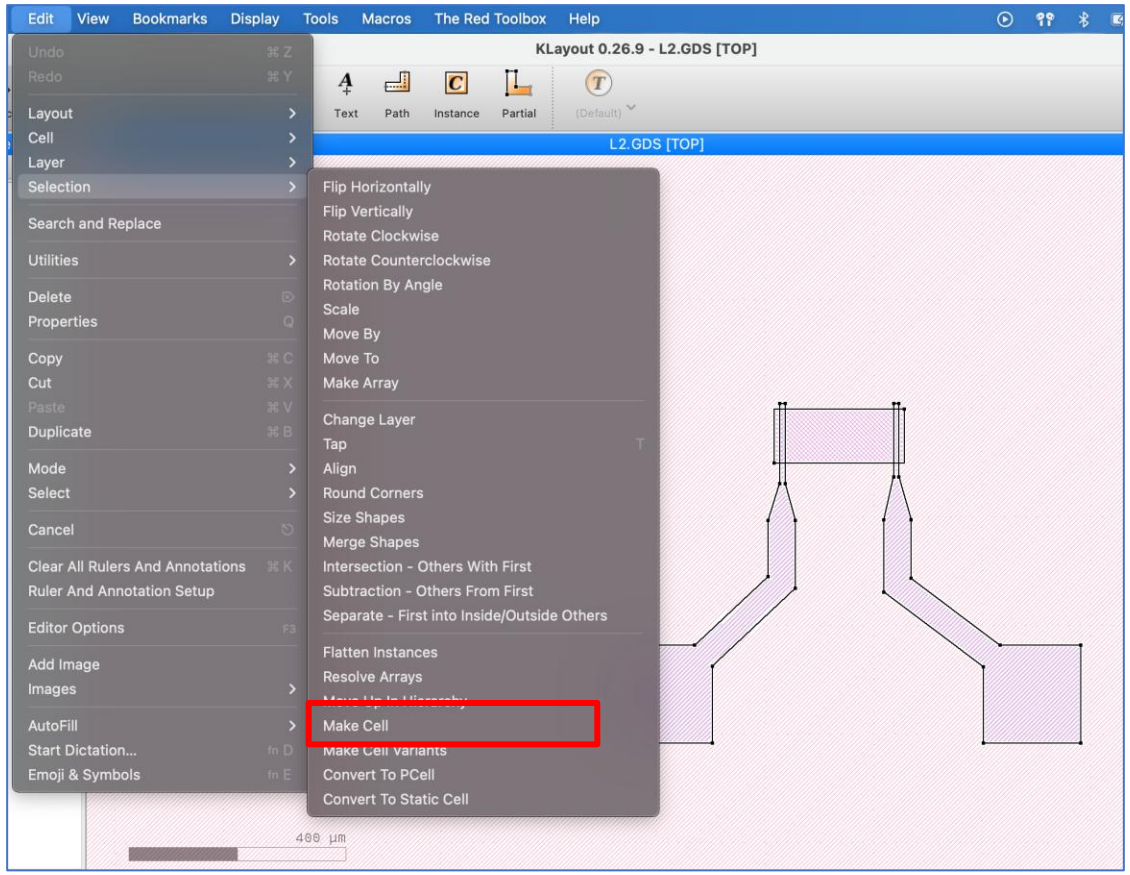
Select the structure + Edit + Make Array

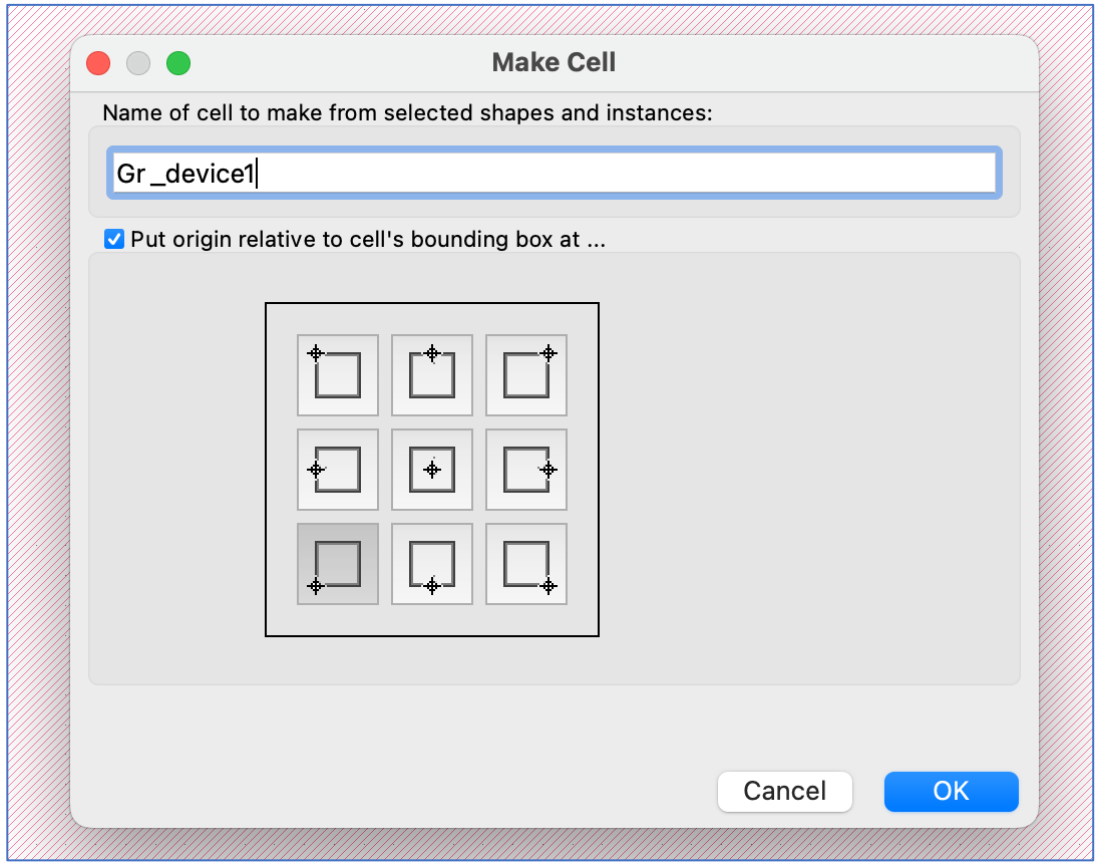


Simple device – Arrays

Option B

Create a “Cell” and use command “Instance”

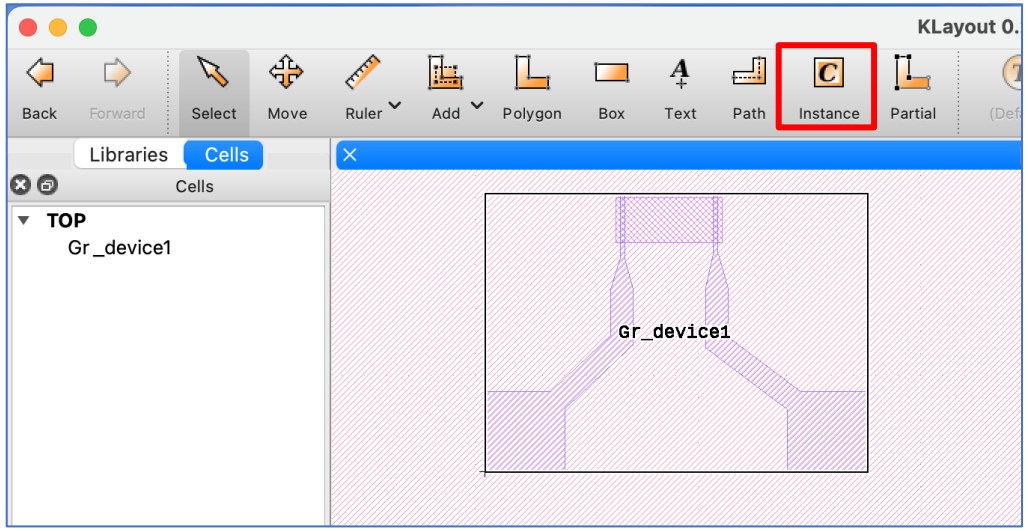


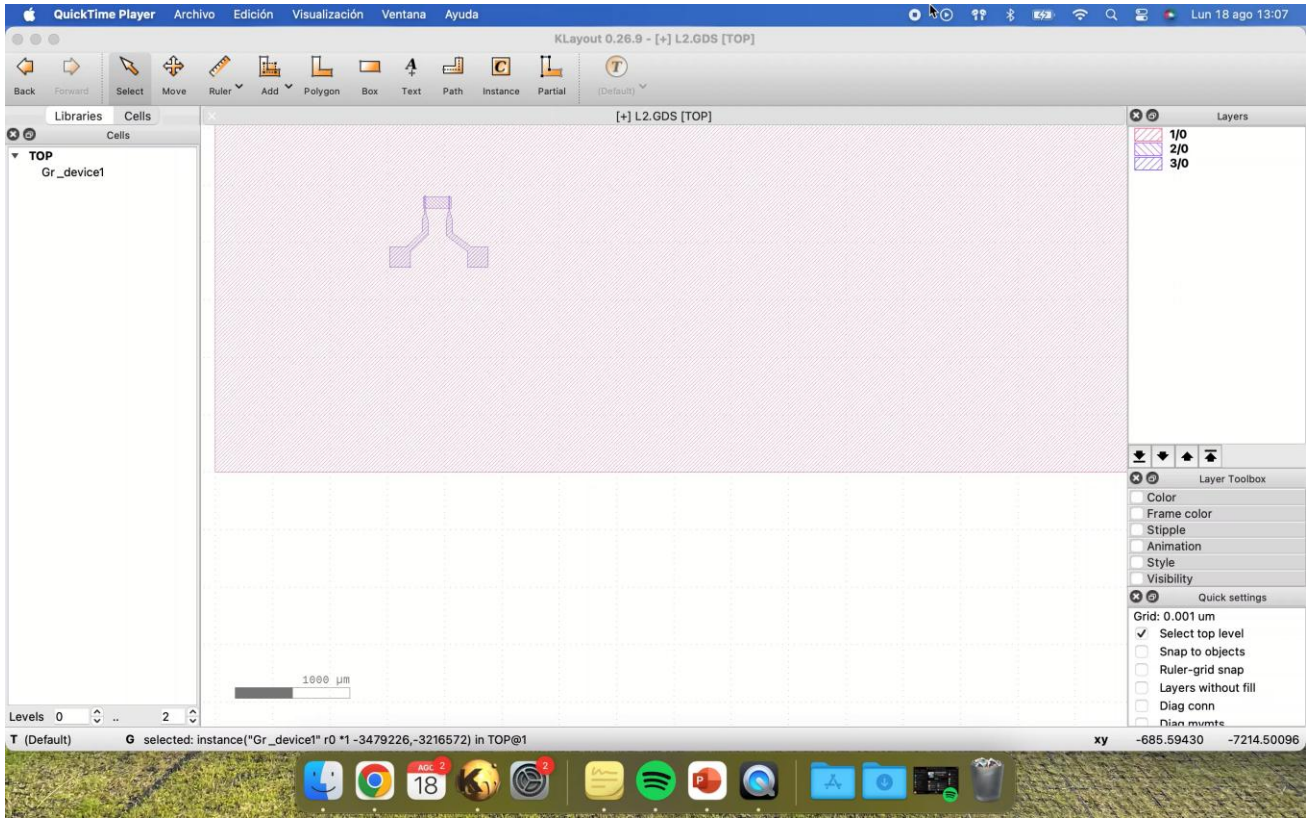


Simple device – Arrays

Option B

Create a “Cell” and use command “Instance”

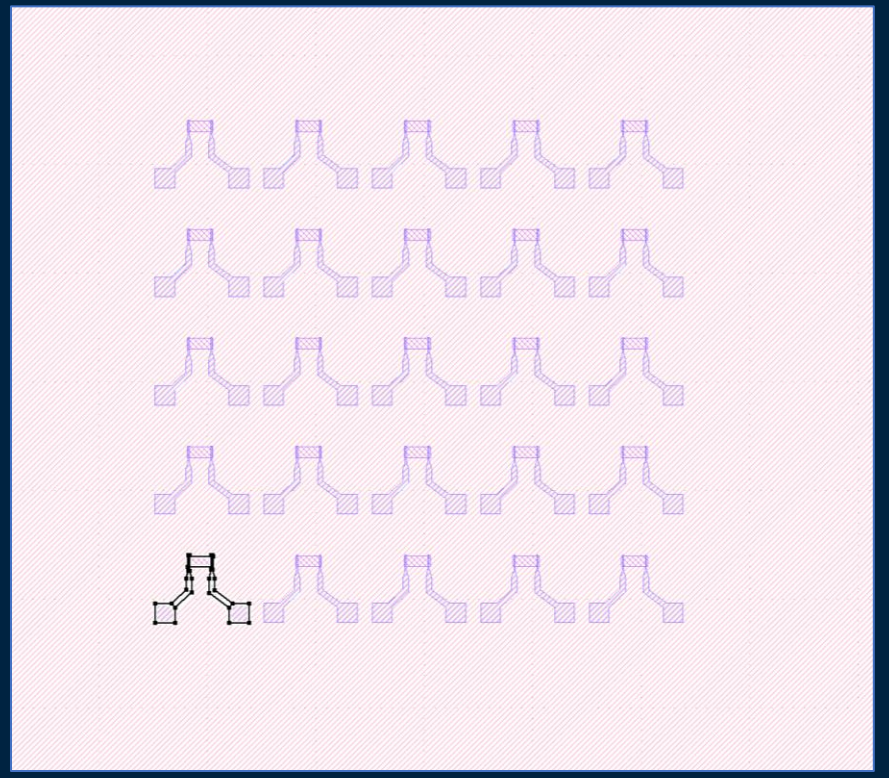




Graphenea

Exercise: Draw a simple GET

- 2 layers
- Contacts and Graphene
- Make an array



2D PILOT LINE

2 November 2026

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the European Union

Design Rule Check

2D PILOT LINE

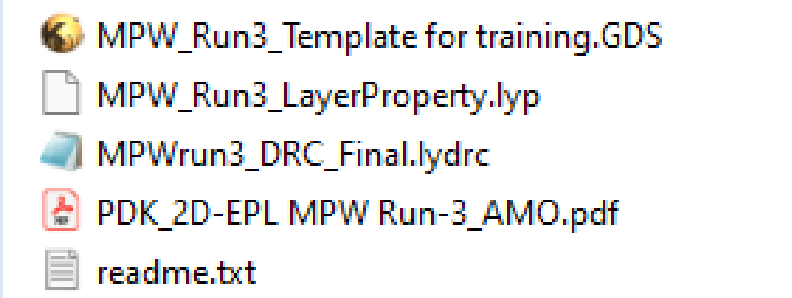
2 November 2026

Funded by
the European Union

Using KLayout with DRC Check

Files provided

- GDS template file
- Layer Name file
- DRC code
- PDK Document
- Readme file for loading and running the DRC file



the DRC files (in phyton) have to stay in the same folder as the design

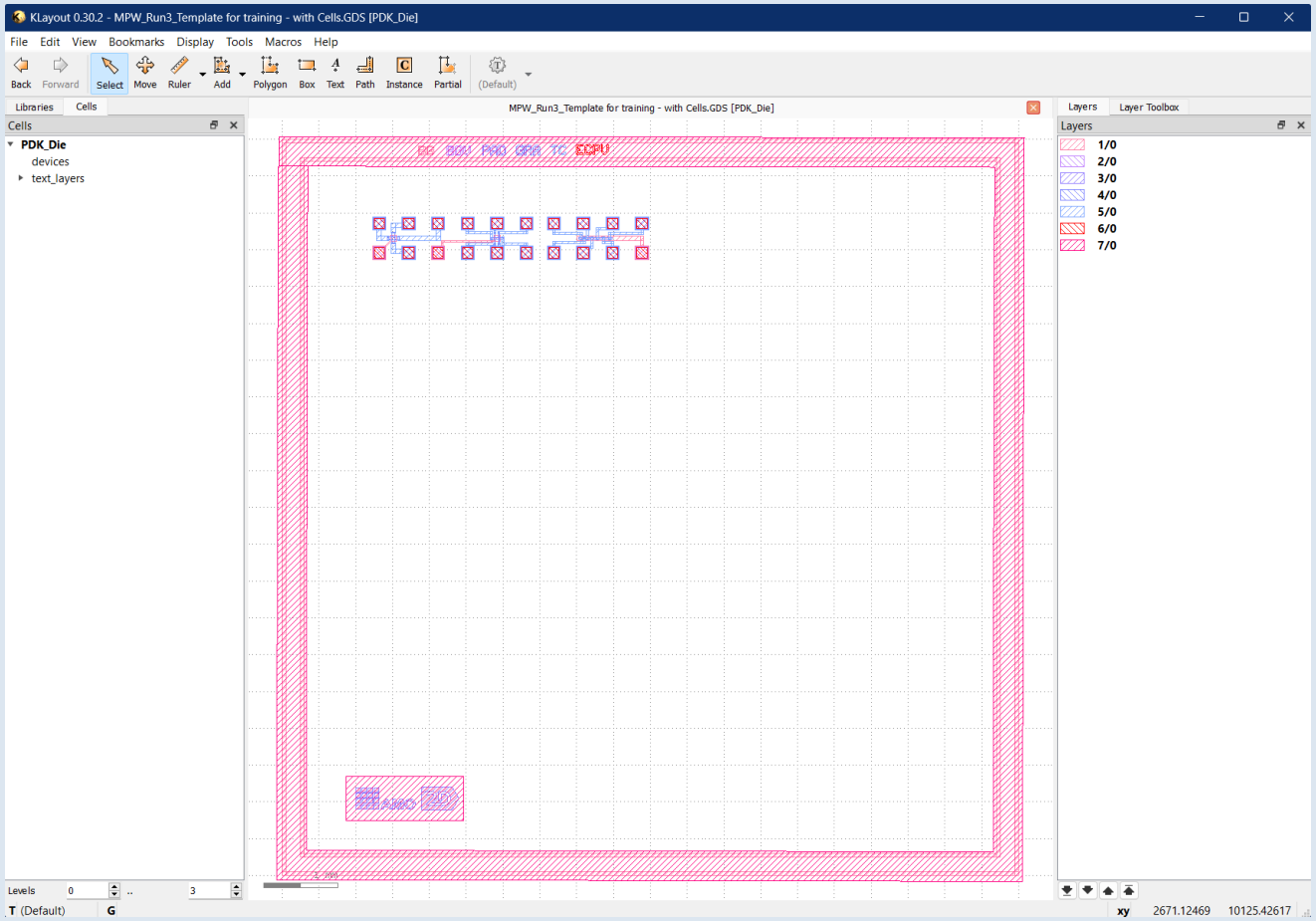
How to run the DRC script:

1. Open the MPW_Run3_Final (GDS file)
2. File - Load layer Properties - load the file: MPW_Run3_LayerProperty.lyp
3. In Macros - Macros Development - In the Ruby Sheet click with the right bottom - add location (add the folder where the file MPWrun3_DRC_Final.lydrc is)
4. Select the file MPWrun3_DRC_Final.lydrc
5. Click in run script.

⇒ **See on the following slides**

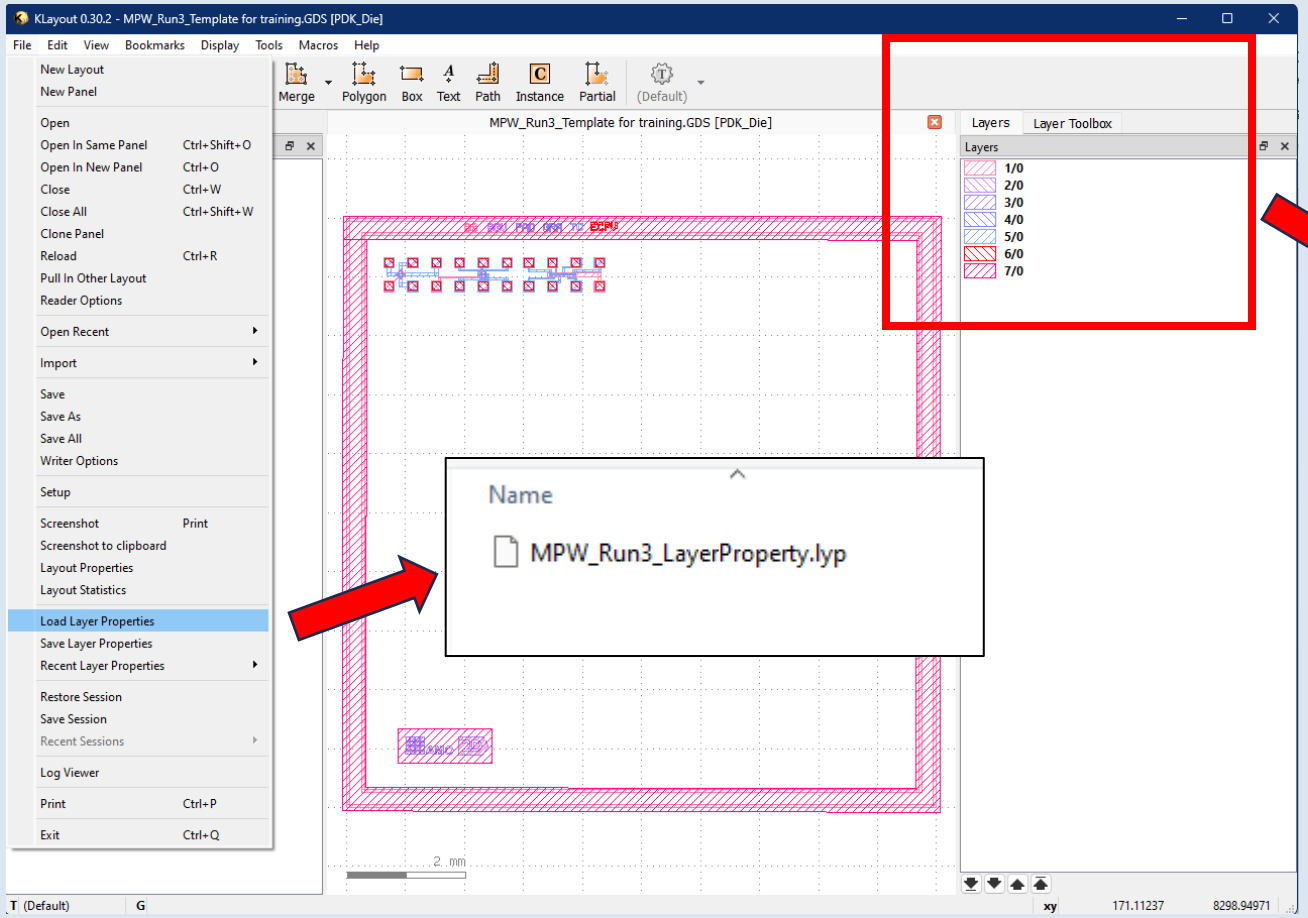
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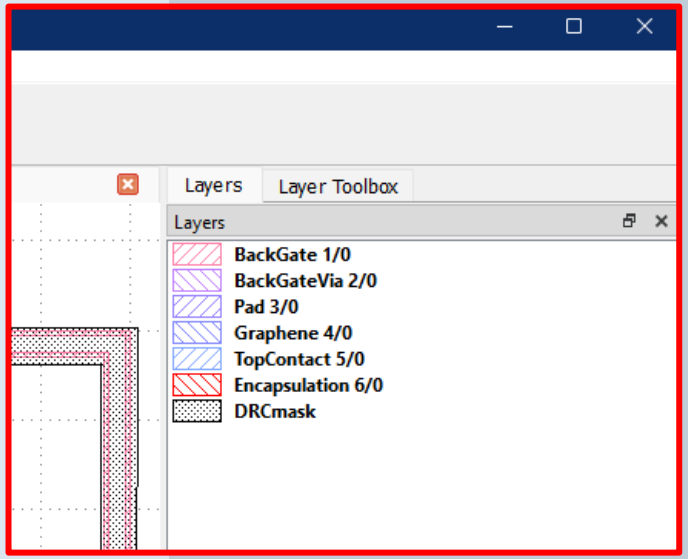
KLayout – 1. Open File



- *Chip size 10x10mm*
- *3 reference devices*
- *7 layers incl. DRC mask for shading the rim*

KLayout – 2. Load layer Properties



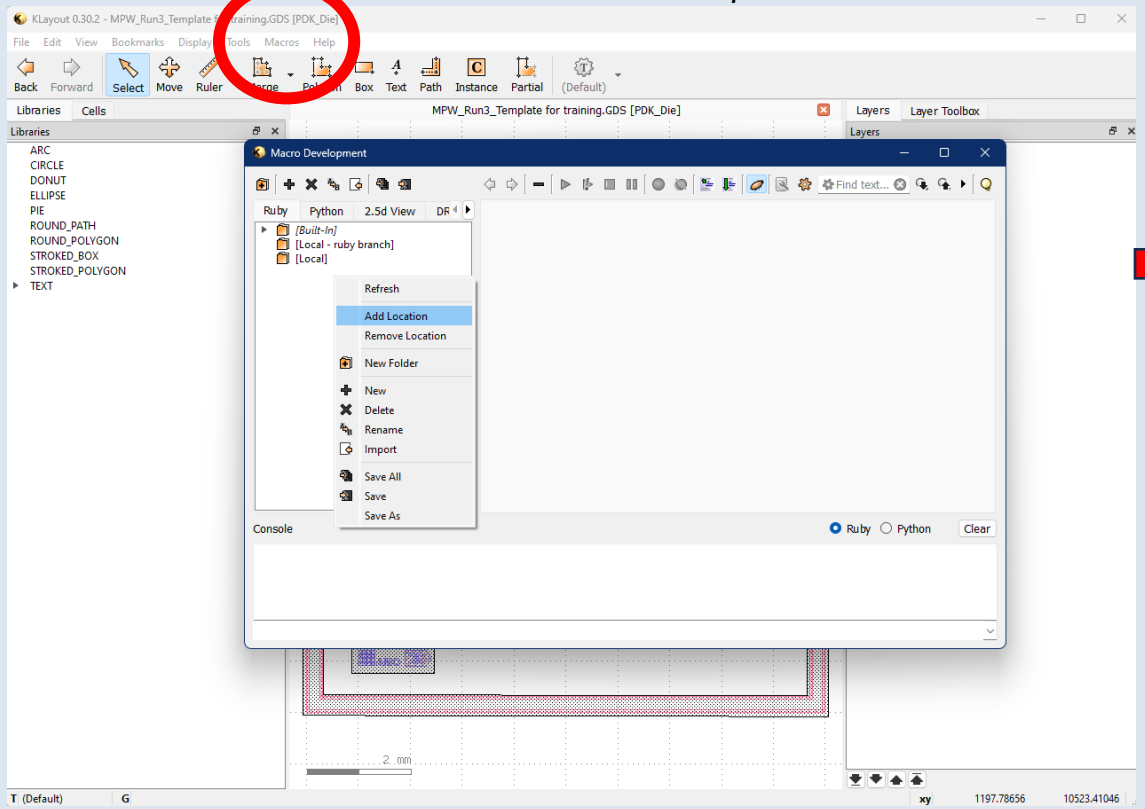


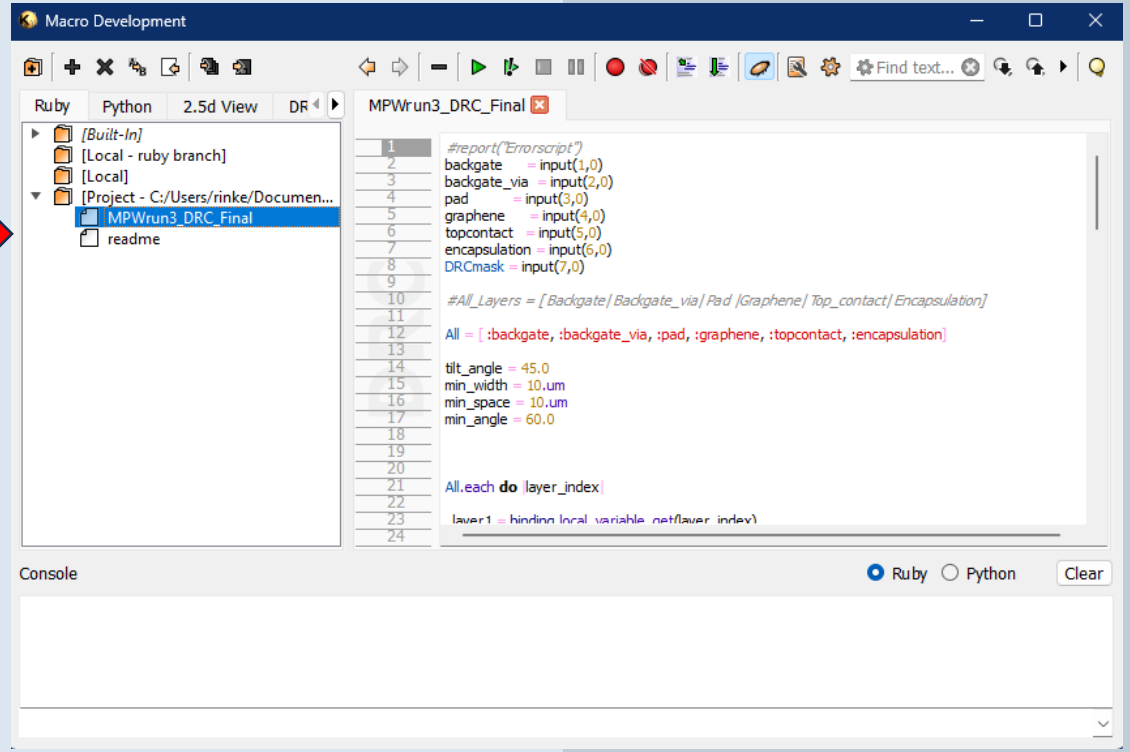
Layers get names and colors for better orientation

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KLayout – 3. Load DRC Script

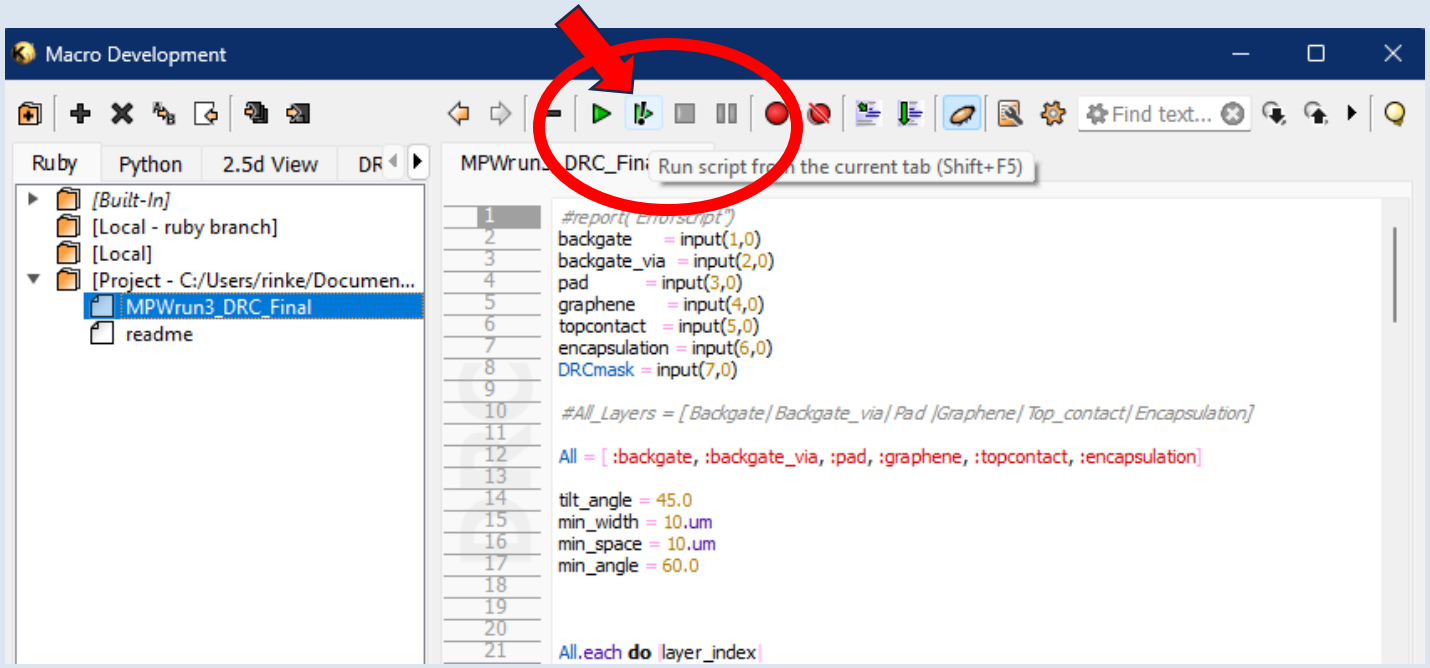
Macros – Macro Development





- *Add the location of the DRC file in the Ruby sheet*
- *Select the DRC file*

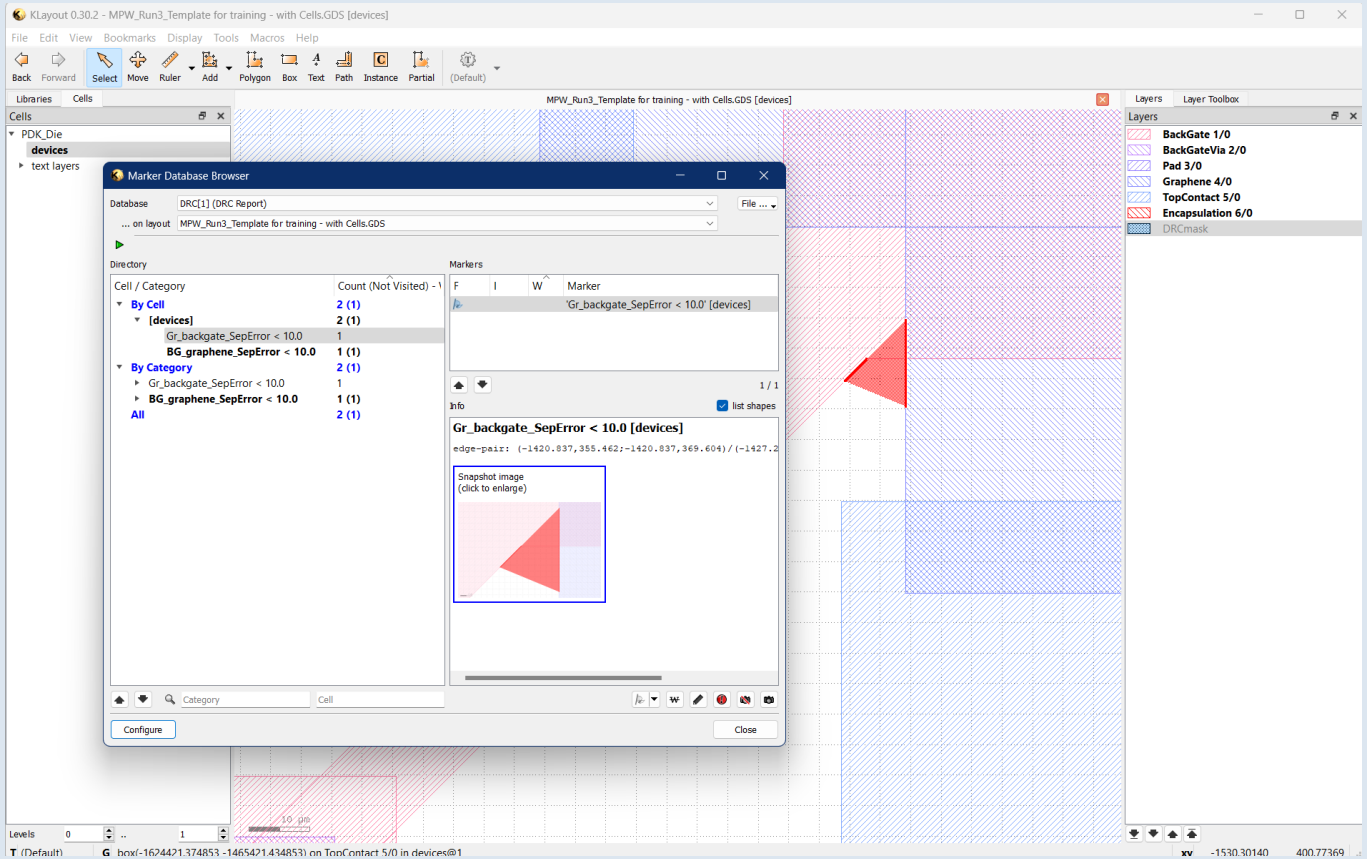
KLayout – 4. Run DRC Script

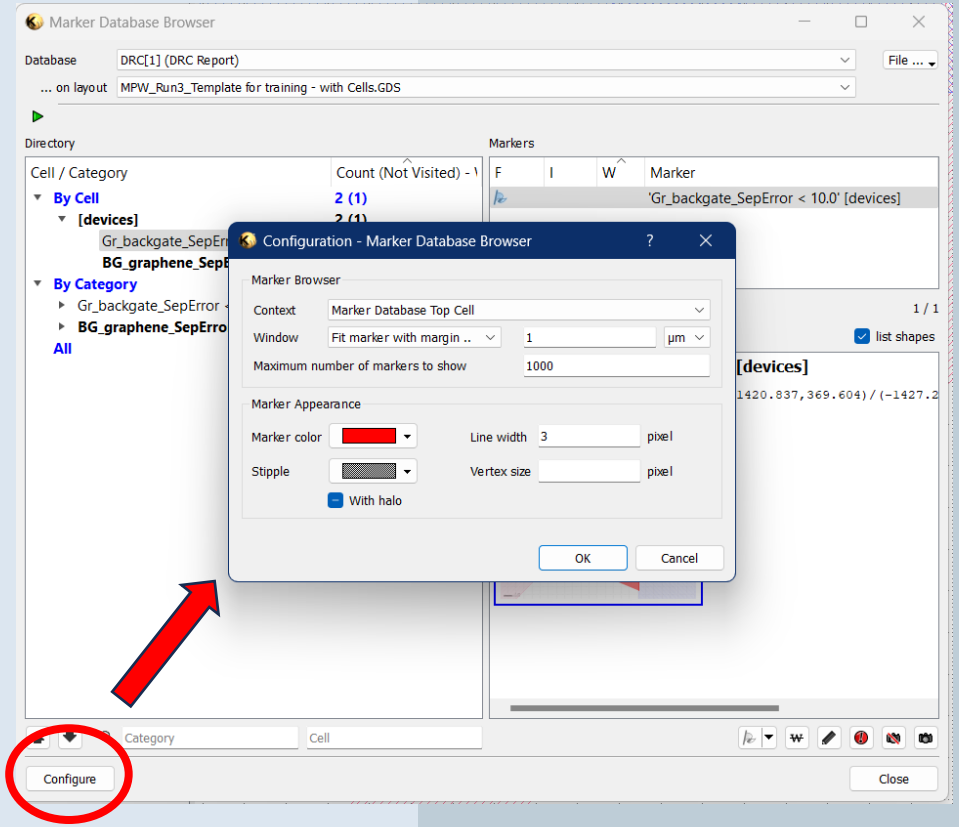


Make sure you selected the device cell ("show as new top")

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KLayout – 5. See Errors

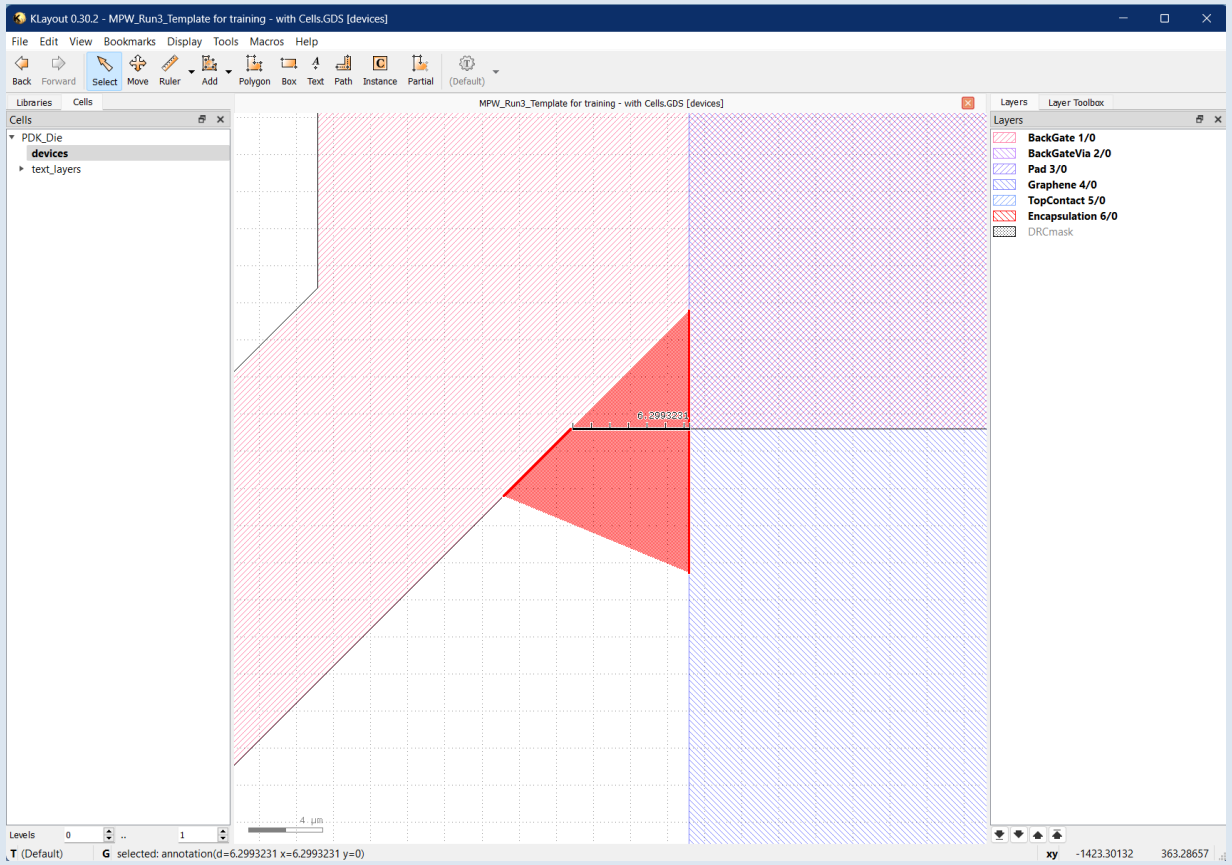




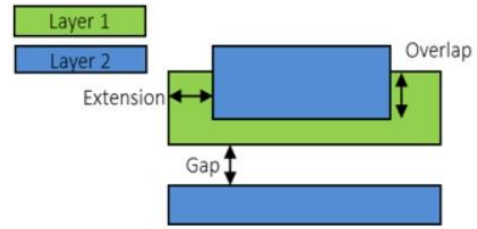
- *Marker Database Browser opens*
- *List of errors by cell and category is displayed*
- *Use configure to adjust marker appearance*

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KLayout – 5. See Errors



Here a separation error according to this rule:

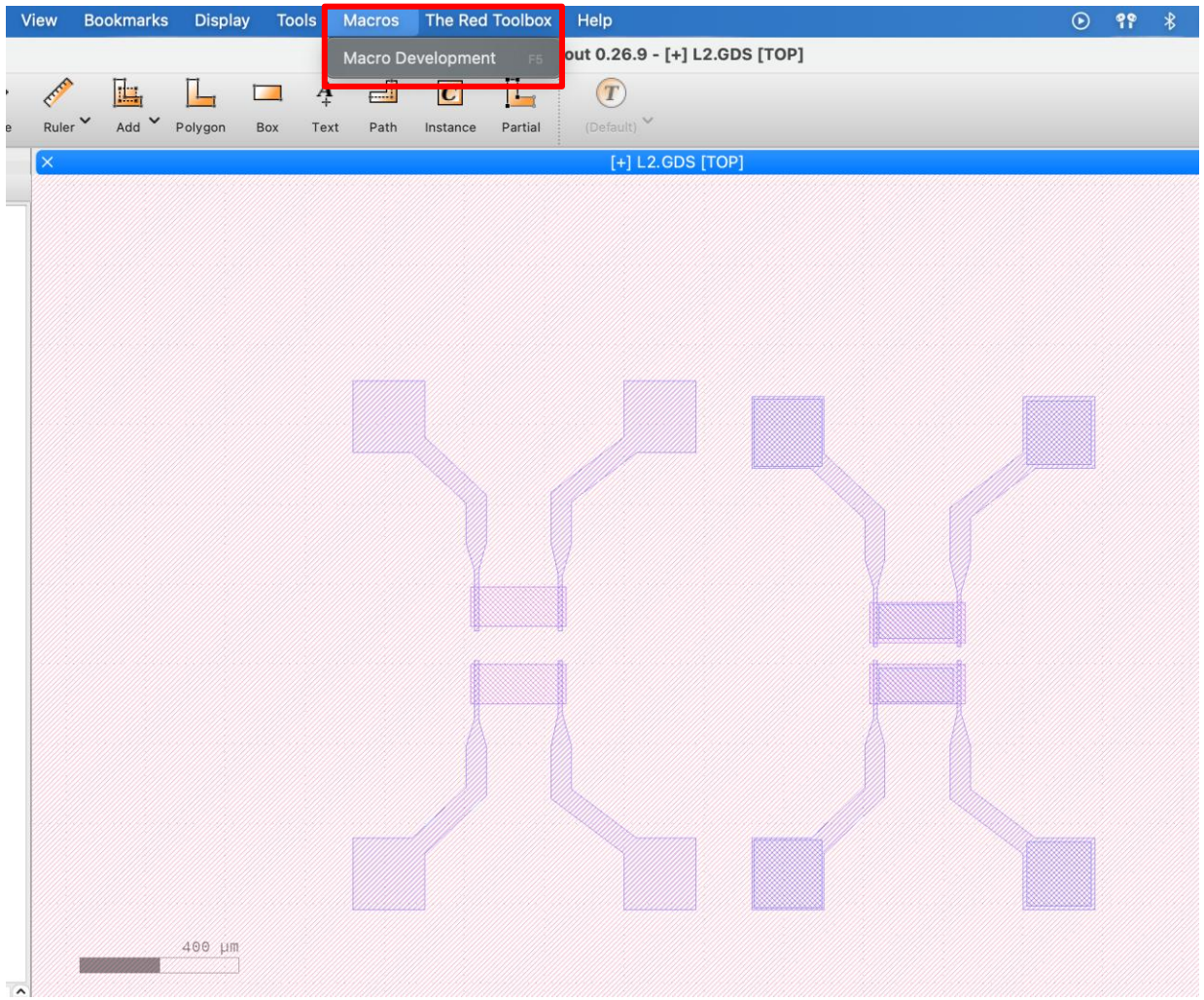


Over-layer tolerance	
Gap	≥ 10 µm
Overlap	≥ 10 µm
Extension	≥ 10 µm

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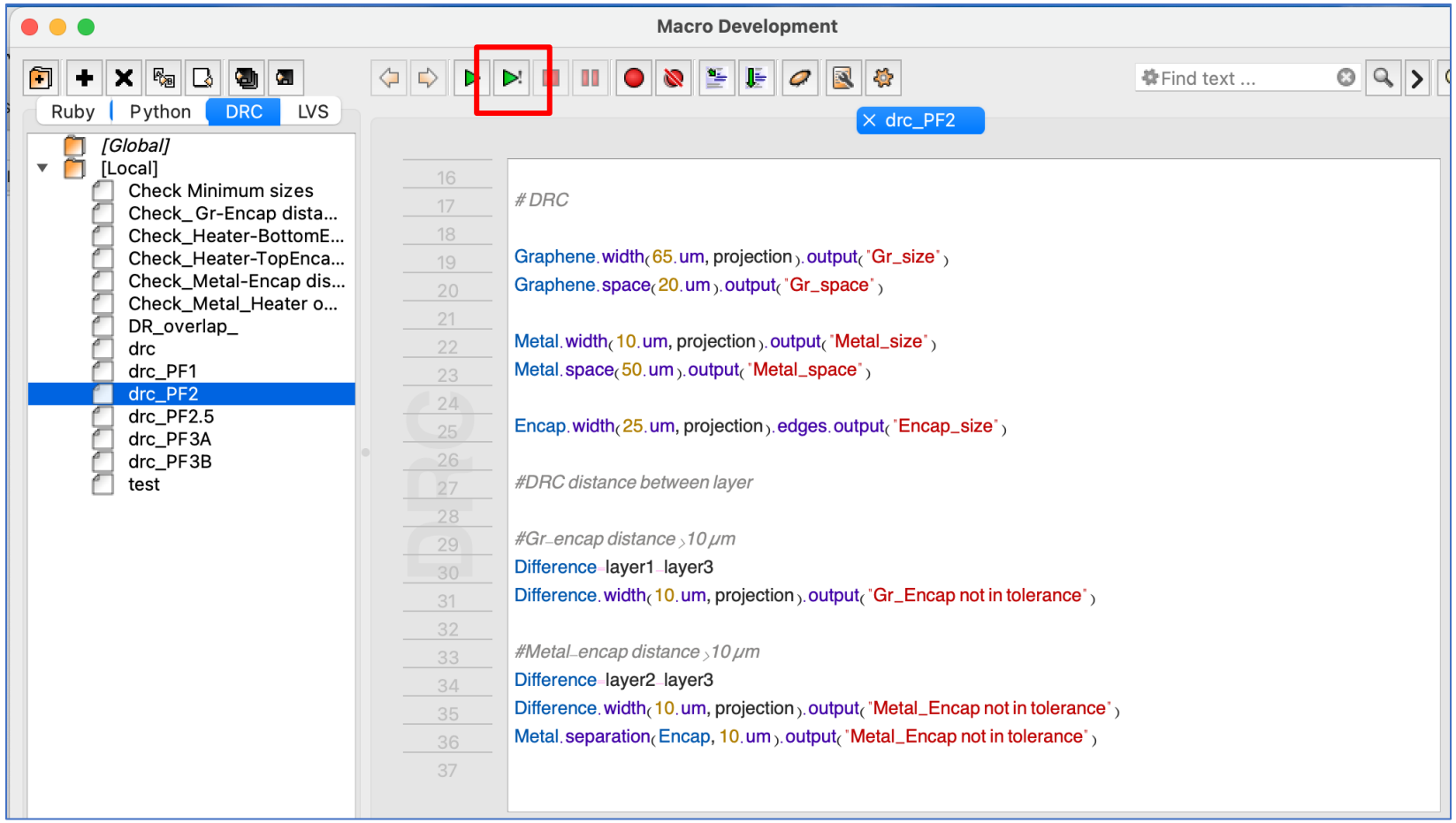
Design rule check

Macros + Macro development



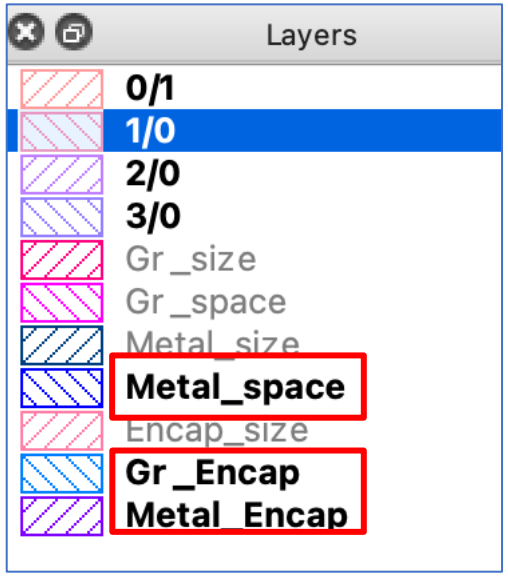
Design rule check

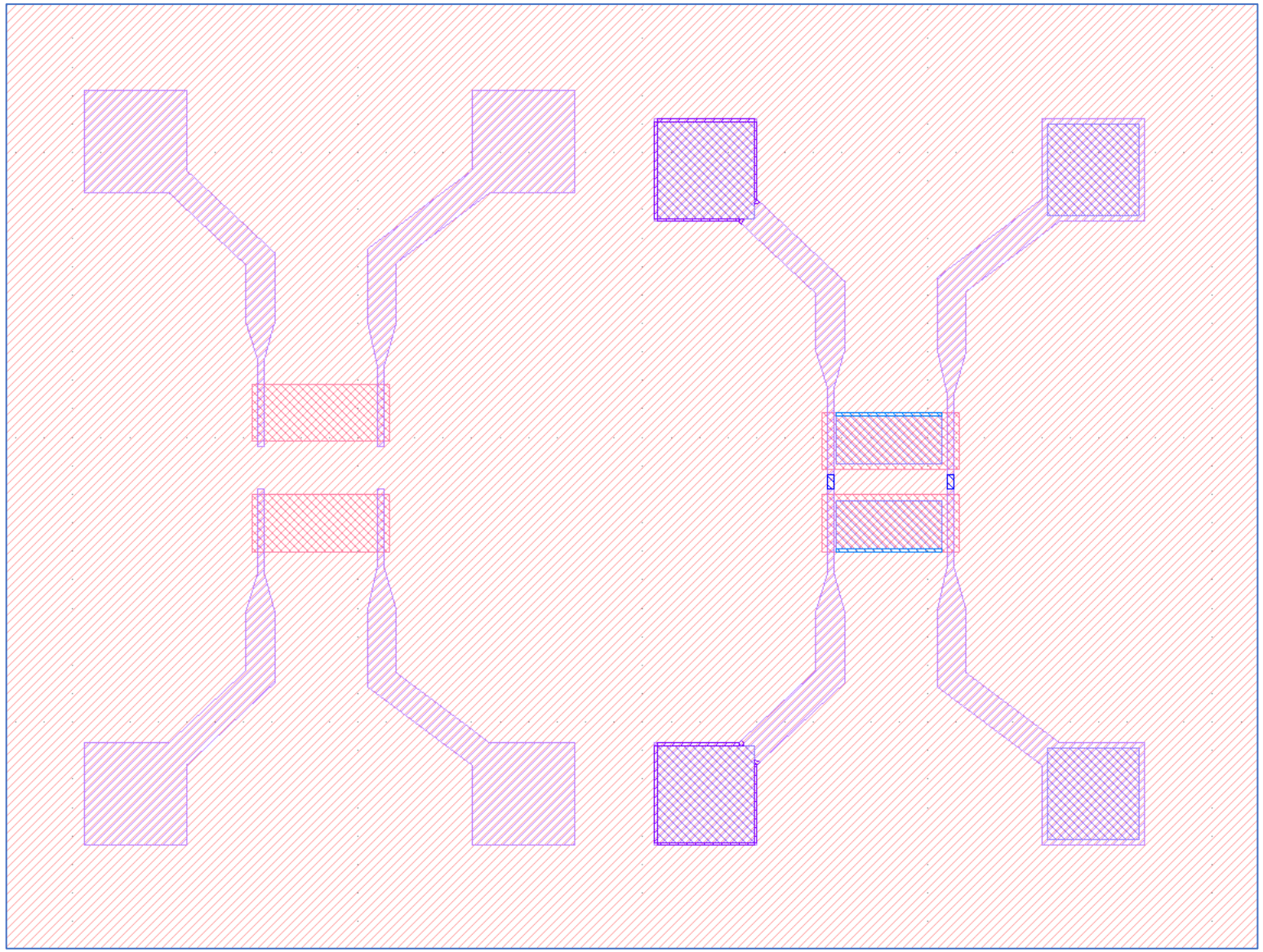
Macros + Macro development



Design rule check

Layers with DR violations

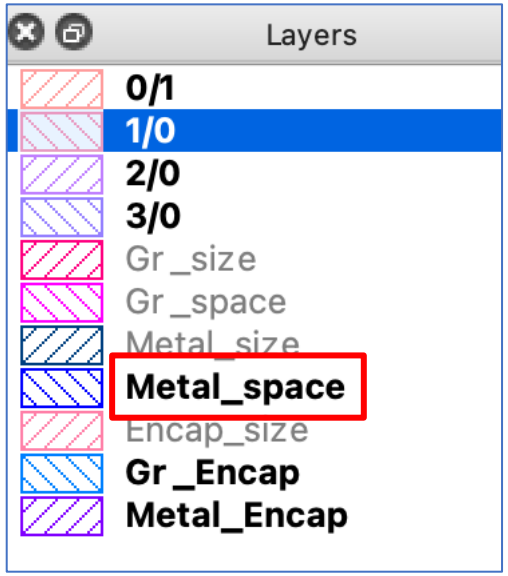


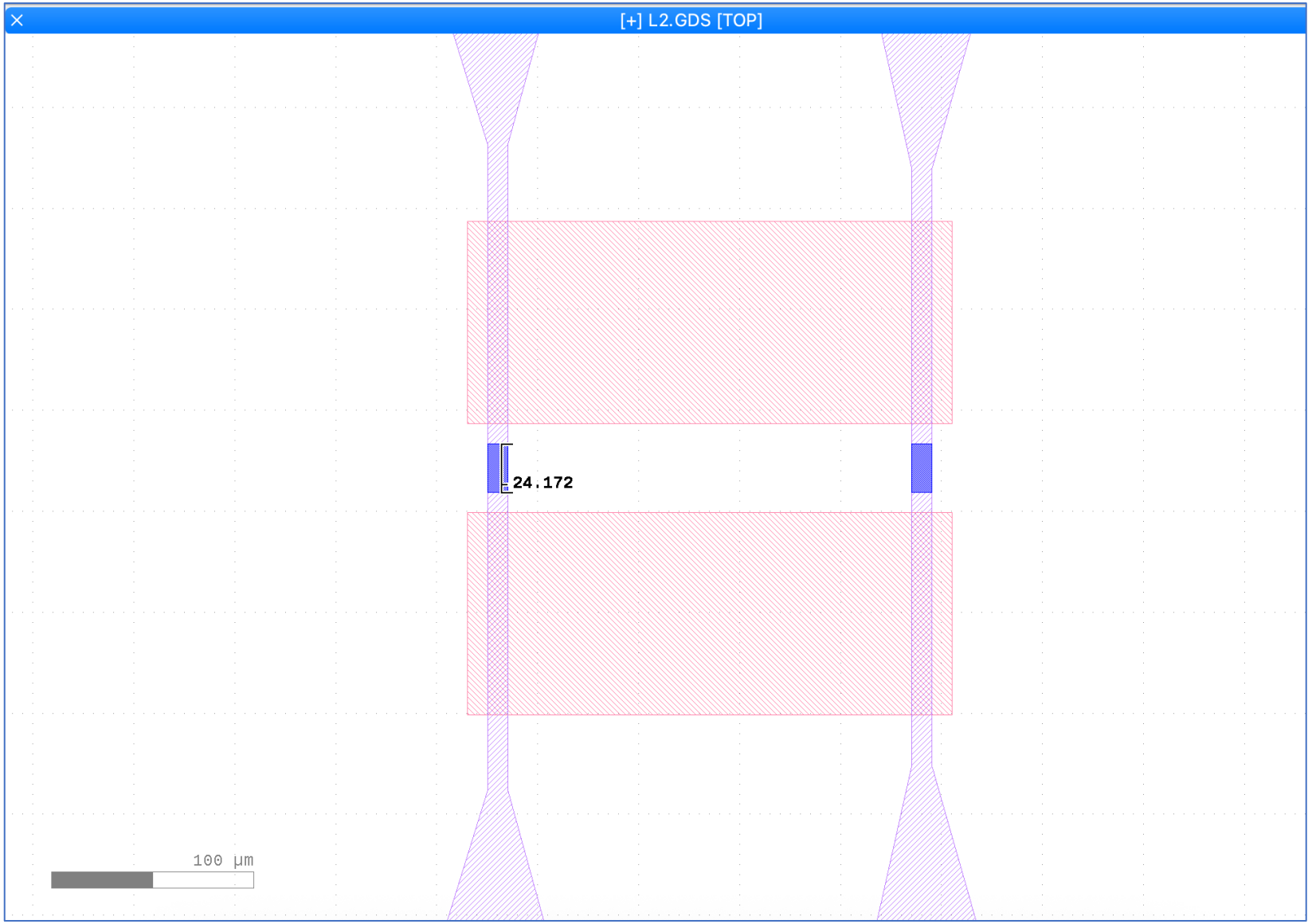


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Design rule check

Metal space

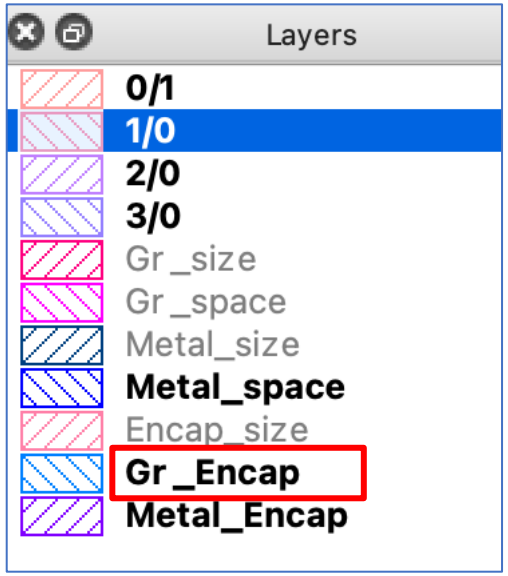


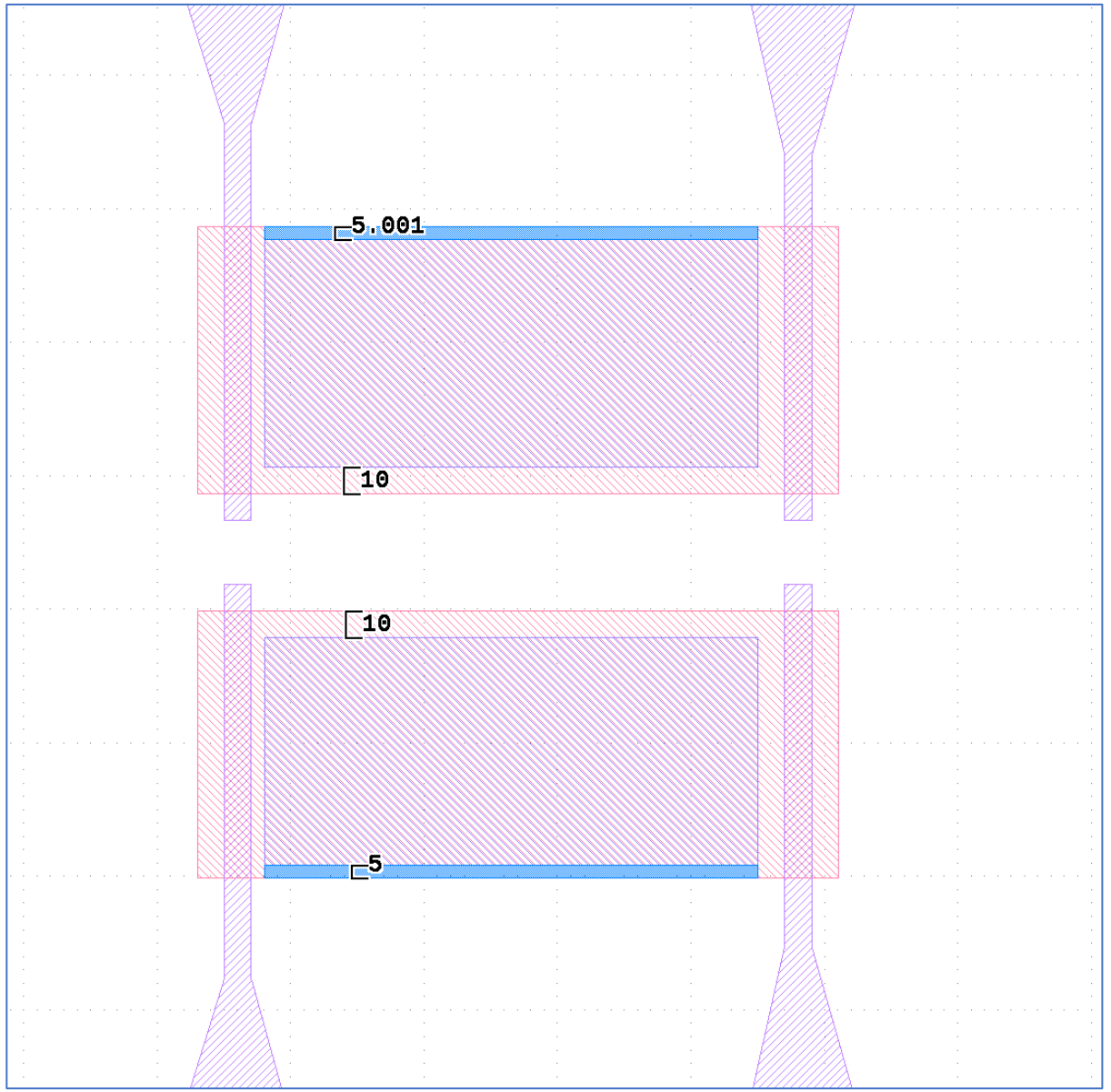


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Design rule check

Layers with DR violations

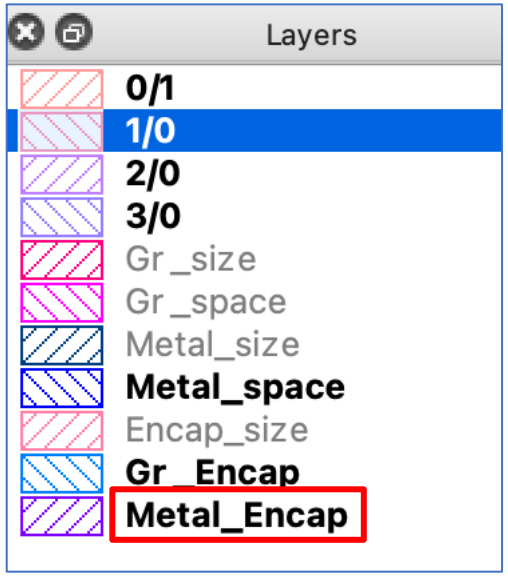


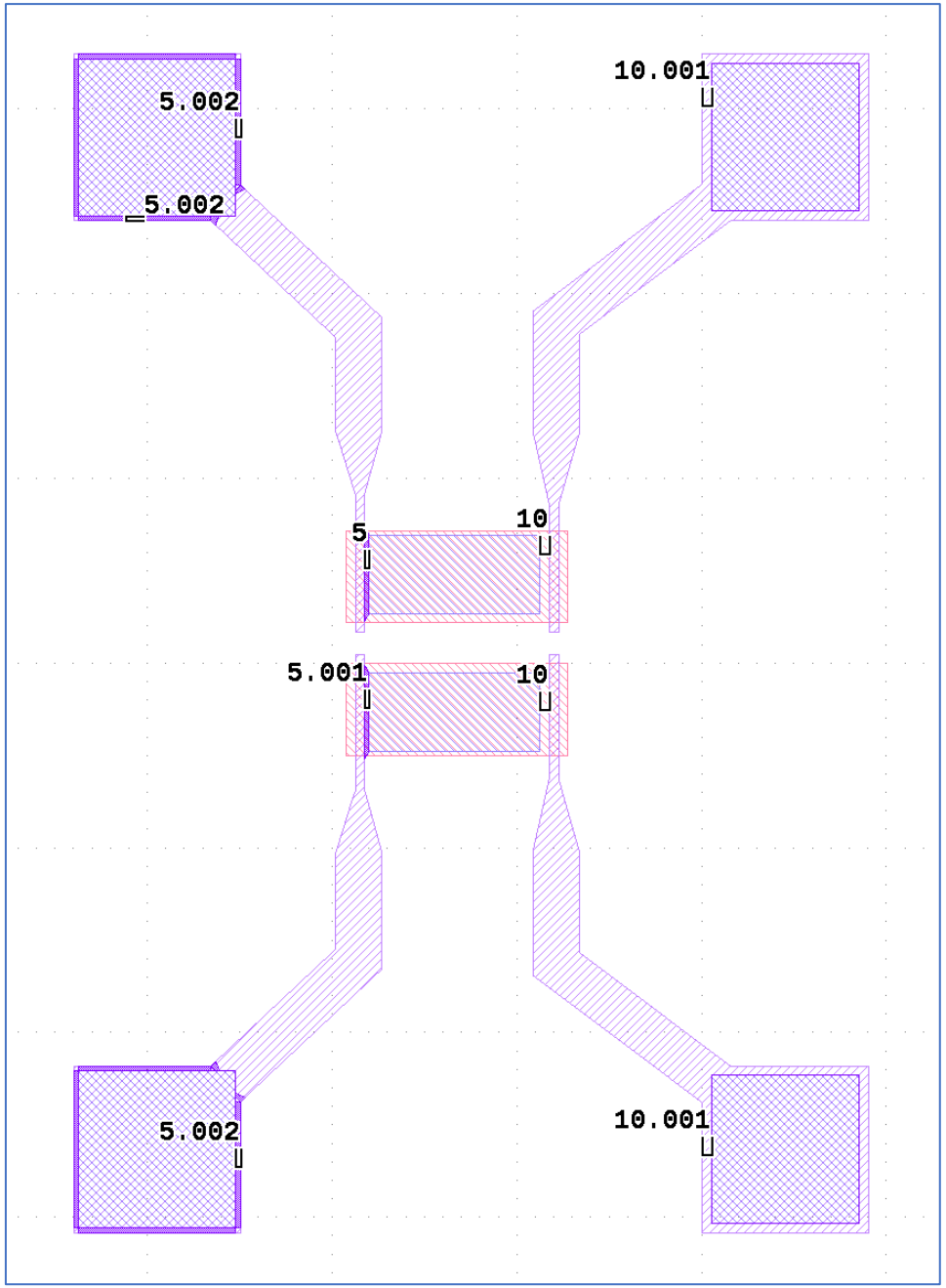


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Design rule check

Layers with DR violations





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Thanks for listening!

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/GrapheneEU

2D PILOT LINE

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