Recent progress in fabrication and electrical evaluation of 2D channel FETs in a 300 mm pilot line

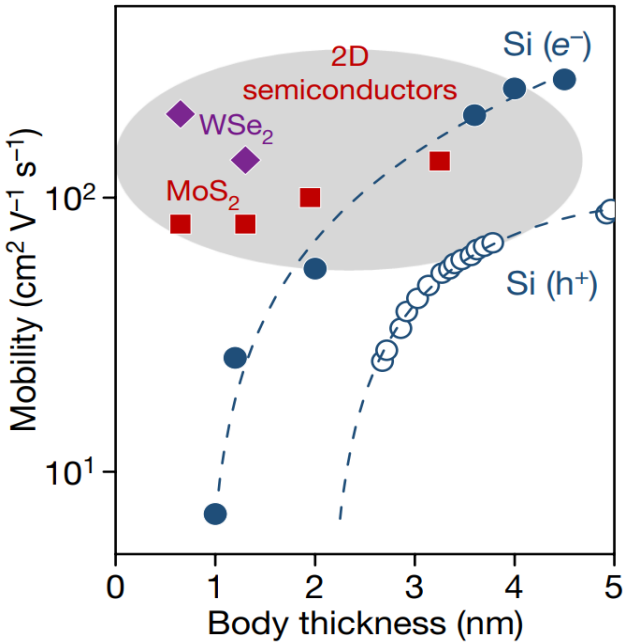
Quentin Smets

02/11/2026

Why 2D materials can extend CMOS roadmap

- High carrier mobility (n & p), in the right conditions (>100 $cm^2/(V \cdot s)$)
- Uniform thickness
  → advantage over thinned bulk materials

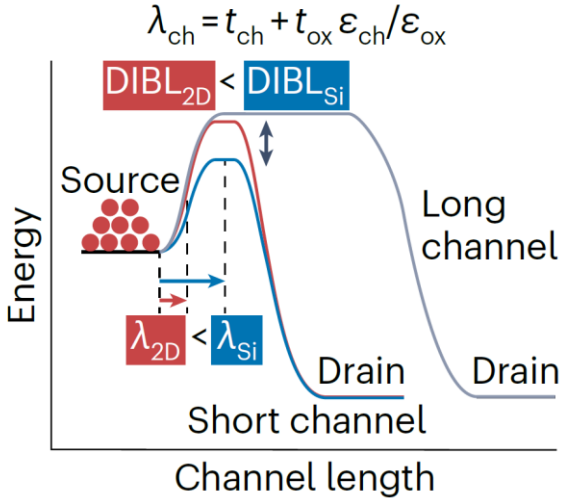
Often in practice (currently):
- low mobility (≤20 $cm^2/(V \cdot s)$)
- nonuniform film with defects

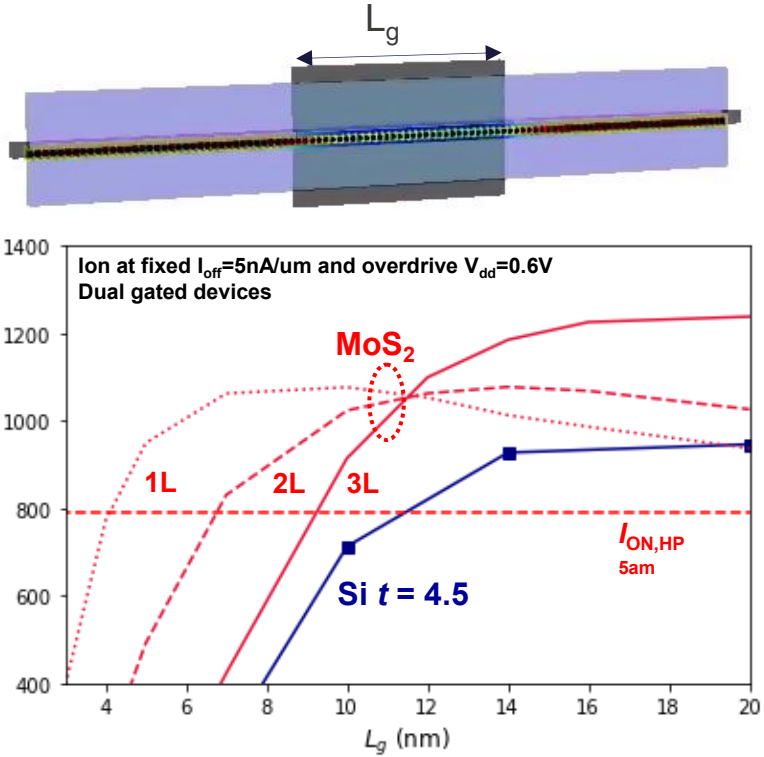


Liu, Y. *et al* (Hunan). *Nature* **591**, 43–53 (2021). doi:10.1038/s41586-021-03339-z

2D materials to extend CMOS roadmap

- Maintain electrostatic control at L_{ch}<10 nm
- Predicted to outperform Silicon FETs at ultra-scaled nodes





Y. H. Kim et al. (Korea univ/Samsung/Seoul univ.), Nat Electron, **8,** 9, pp. 770–783 (2025), doi:10.1038/s41928-025-01448-5
F. Xi et al. (imec), Nature Nano 2026 (accepted) https://arxiv.org/abs/2607.12707

2D materials in imec's logic scaling roadmap

2018	2020	2023	2025	2027	2029	2031	2033	2035	2037	2039
N7	N5	N3	N2	A14	A10	A7	A5	A3	A2	sub-A2

DEVICE AND MATERIAL INNOVATIONS

	FinFET			NanoSheet			CFET			2DFET, ?, …	
	Introduction	Scaled	Extended	Introduction	Scaled	Extended	Introduction	Scaled	Extended	Introduction	Scaled
Metal Tracks	6	6	6	5	5	5	4	<4	<4	<4	<4

CONTINUED DIMENSIONAL SCALING

		0.33NA EUV			0.55NA EUV				0.75NA EUV		
Metal Pitch [nm]	40	28	23	22	21	18	18-16	18-14	16-12	16-12	14-10

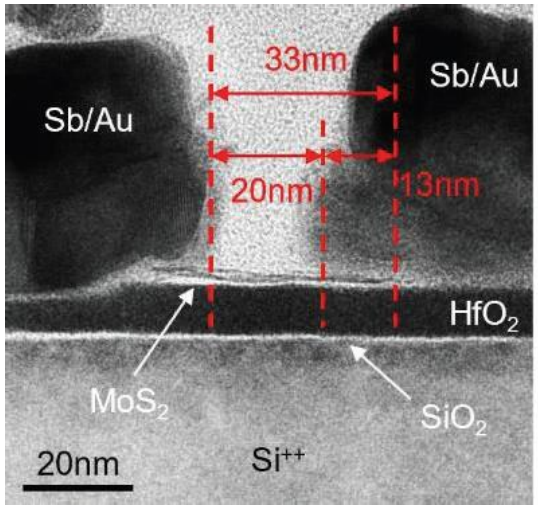
CHIP INTERCONNECT ARCHITECTURE

				Back-side Power - Global interconnects			Back-side Power - Local signal lines				
Back-side Metal Pitch estimate [nm]		-	-	160-65	115-45	90-42	40-34	40-28	tbd	tbd	…

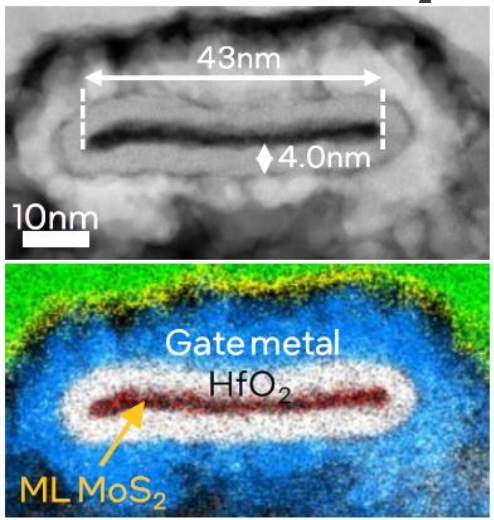
Main challenges for TMD FETs in state of the art

- Channel defectivity
  - Point defects, grain boundaries
  - Growth, transfer, cleaning
- High contact resistance
  - often Schottky-type
- Gate stack
  - EOT, uniformity, defectivity
- Advanced integration
  - Doping
  - Selective etch
  - Spacers

Back gated MoS_2

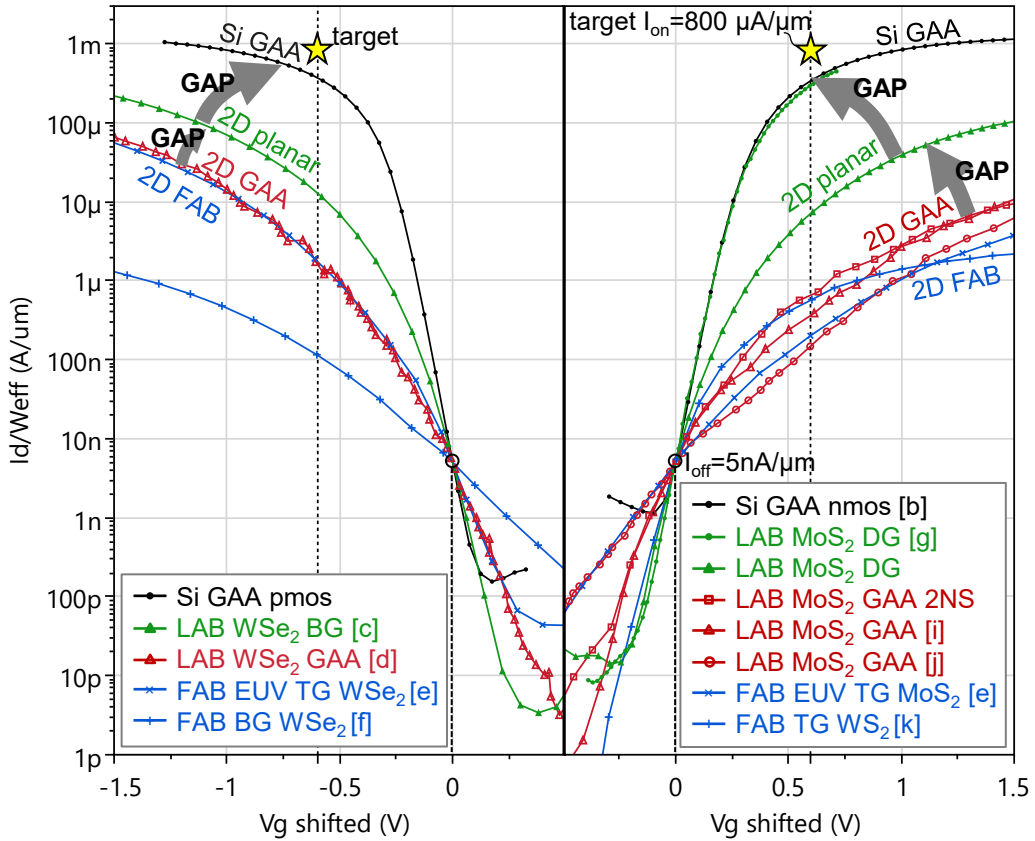


Gate-all-around MoS_2

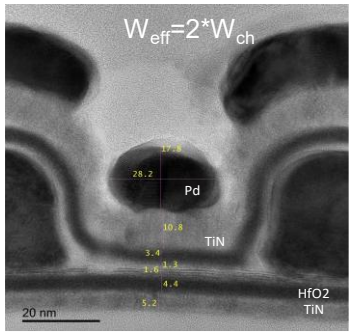


W.-C. Wu *et al. (TSMC)*, VLSI (2024). doi:10.1109/VLSITechnologyandCir46783.2024.10631401.
W. Mortelmans *et al. (intel)*, VLSI, (2024), doi:10.1109/VLSITechnologyandCir46783.2024.10631395.
K. S. Kim *et al.* (MIT,Samsung), Nature Nanotechnology, **19**, 7, pp. 895, (2024). doi:10.1038/s41565-024-01695-1.

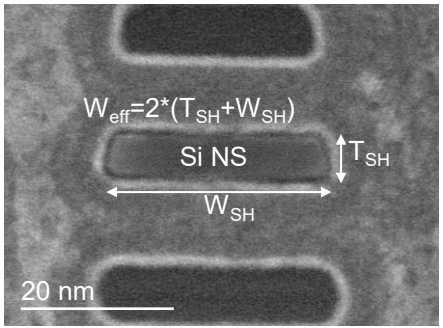
Benchmarking I_{on} at fixed overdrive highlights on-current challenge



LAB MoS2 nFETs



Si nanosheet GAA



[b] A. Vandooren et al, IEDM (2025)
[c] T. D. Ngo et al., IEDM (2025)
[d] M. Jaikissoon et al., VLSI (2025)
[e] T. Schram et al., VLSI (2026)
[f] C. Dorow & T. Schram et al., IEDM (2023)
[g] J. Jiang et al., MoS2 Nat. Elec. (2024)
[i] W. Mortelmans et al., VLSI 2024
[j] B.-J. Chou et al., Nanotechnology, vol. 35, no. 12, (2024)
[k] T. Schram & Q. Smets et al., Disc. Elec. vol. 3, no. 1, p. 15, (2026)

Biggest challenge in 2D for logic:
Improving I_{on} at V_{off}+0.6V

At imec: three Industrial CVD Reactors for TMD Materials

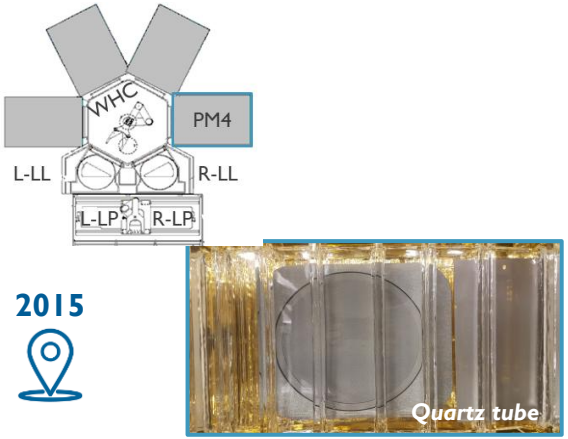
MOCVD chemistry from metal-hexacarbonyl & H_2S precursors is the workhorse at imec

Two horizontal CVD reactors | *Close coupled showerhead reactor*

200 mm, Polygon8200

Template focus

- *Epitaxial MoS_2 and WS_2 on sapphire by MOCVD from $M(CO)_6$ & H_2S*
- *Performance demo*

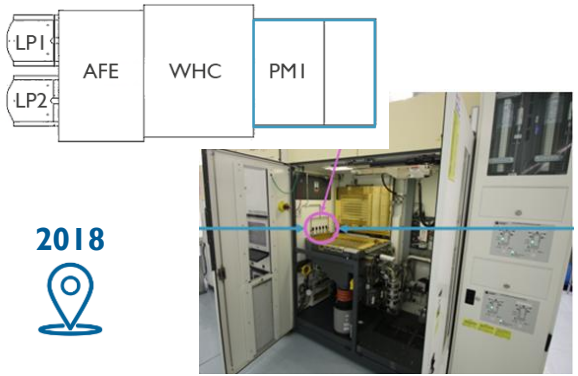


2015

300 mm, Epsilon3200

Direct growth focus

- *MoS_2 and WS_2 MOCVD from $M(CO)_6$ & H_2S*
- *Deposition concepts for T-sensitive architectures*
- *Explore reaction chemistry*



2018

300 mm, Hyperion-I

Template focus

- *MoS_2 and WS_2 MOCVD from $M(CO)_6$ and S precursors*
- *Pathfinding 200 mm & 300 mm sapphire*
- *Performance demo on large-area sapphire substrates*



2023

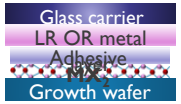
GRAPHENE FLAGSHIP
Funded by the European Union
2D-EPL

imec

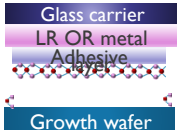
B. Groven et al.(imec), *MRS Fall* 2023, Boston, MA

300 mm scale transfer with rigid carries is viable integration route

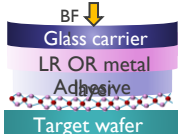
Temporary bond with growth wafer



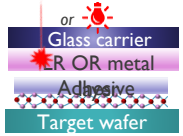
Mechanical debond



Permanent bonding to target wafer



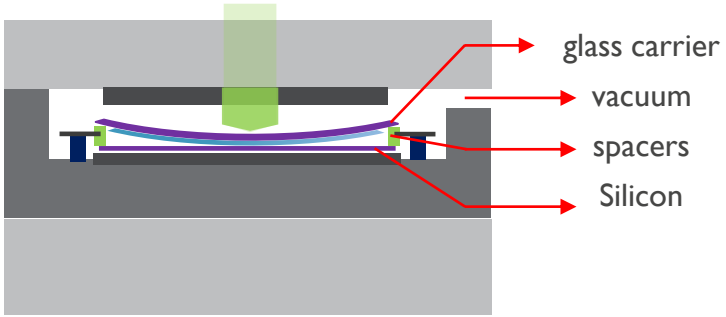
Adhesive release



Adhesive cleaning

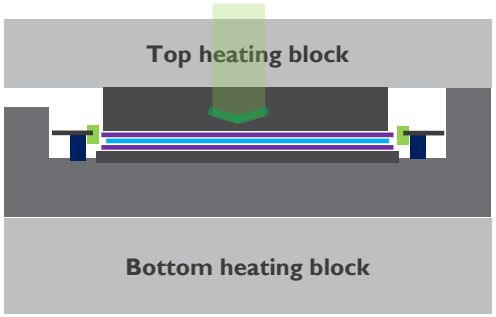






1. Bond front initiation step

- Mitigates the formation of voids
- Improves bonding uniformity



2. Bonding step

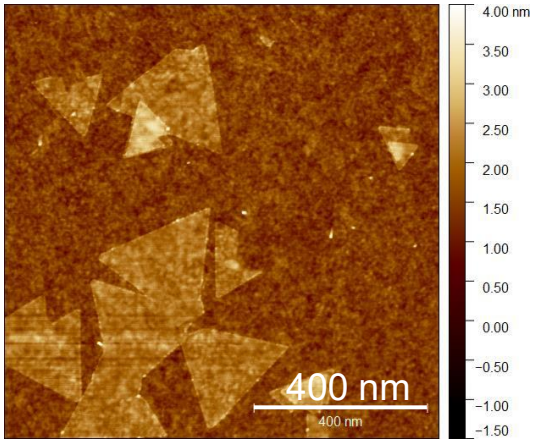
- High pressure (4500N) and elevated T(220°C) allows adhesive reflow
- Greater adhesion
- Reduces stress on MX_2

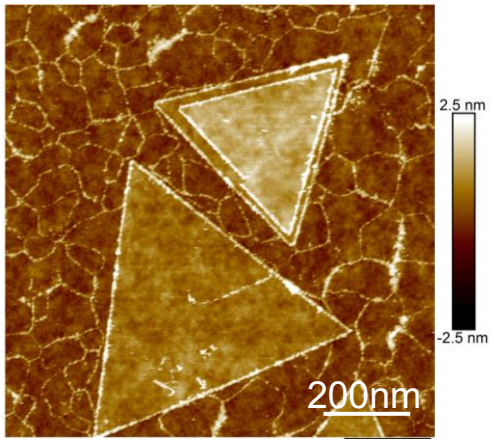
- Fab-compatible & semi-automated on 300mm tools
- Low thermal budget (~250°C)
- No significant center-to-edge and wafer-to-wafer variation
- No observable wrinkles or cracks
- Wafer-to-wafer reproducibility

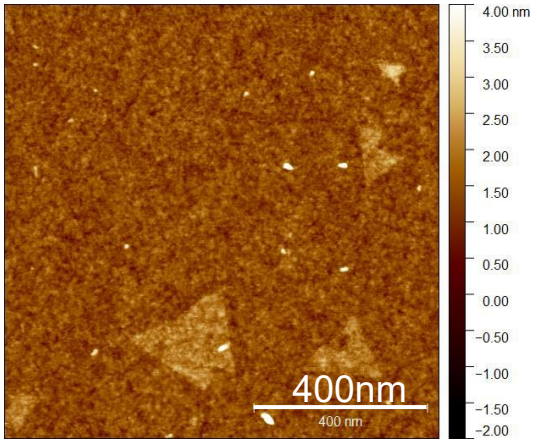
S. Ghosh et al.(imec), *VLSI* (2024) doi:10.1109/VLSITechnologyandCir46783.2024.10631364

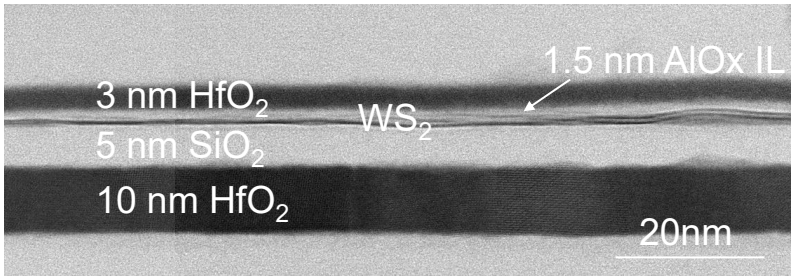
TMA soak method to form highly uniform Al_2O_3 interlayer

Pristine WS_2 film on SiO_2 → "Regular" ALD nucleation fails → "TMA soak" for uniform Al_2O_3 IL









- Tri-methyl-aluminum precursor soak
- Uniform Al_2O_3 IL (1 to 1.5nm) over full 300 mm wafer
- Continue with deposition of thin HfO_2 cap

T. Schram & Q. Smets et al. (imec), *Discov Electron* **3**, 15 (2026) doi:10.1007/s44291-026-00164-4

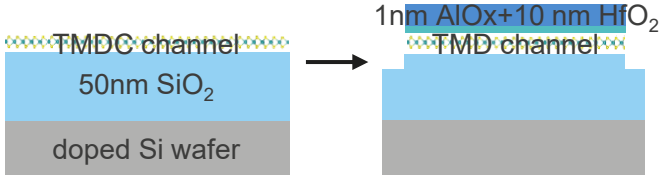
Imec 300 mm integration flow for TMDC FETs (baseline)

- 300 mm Si wafer
- back gate stack dep.
- TMDC dep./transfer

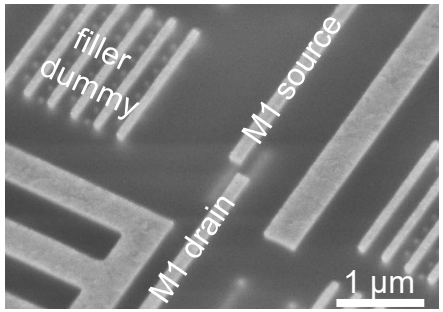
- Al2O3 IL (TMA soak)
- HfO_2 cap (ALD)
- Active patt. (SoC/SoG)

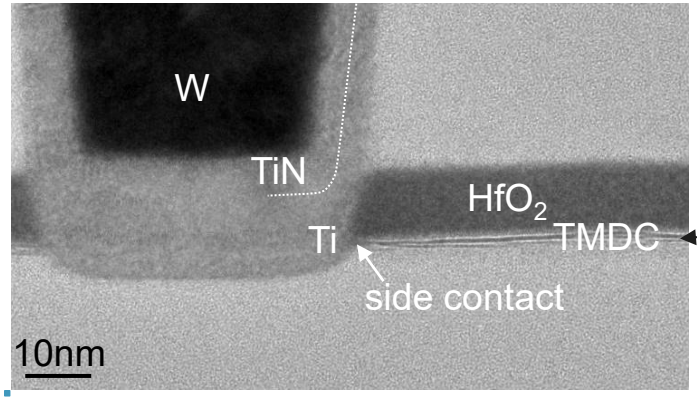
- SiO2 encapsulation & CMP
- M0 side contacts by damascene process

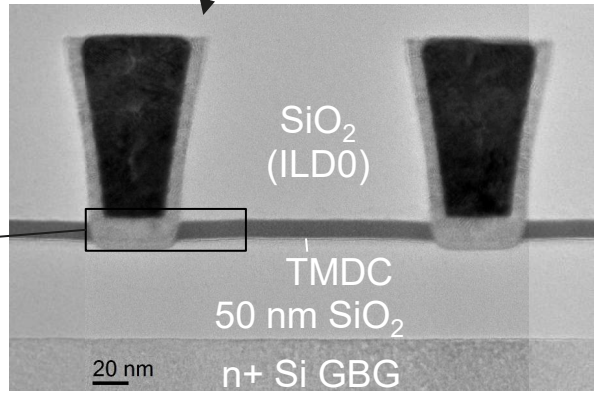
- V0 damascene
- M1 damascene
- backside metal

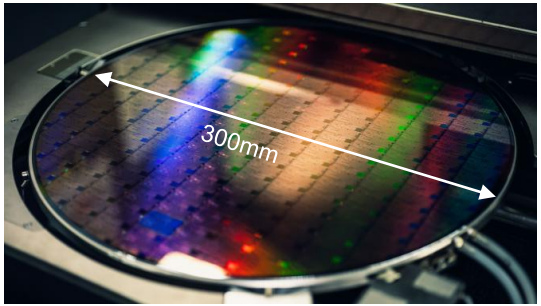


Top view:







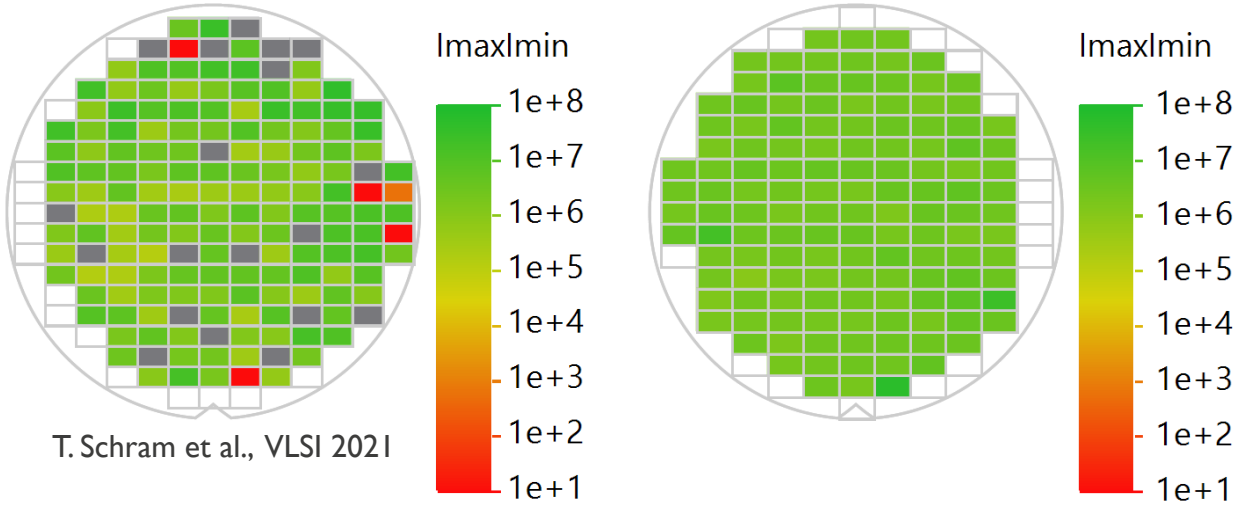


T. Schram & Q. Smets et al. (imec), *Discov Electron* **3**, 15 (2026) doi:10.1007/s44291-026-00164-4

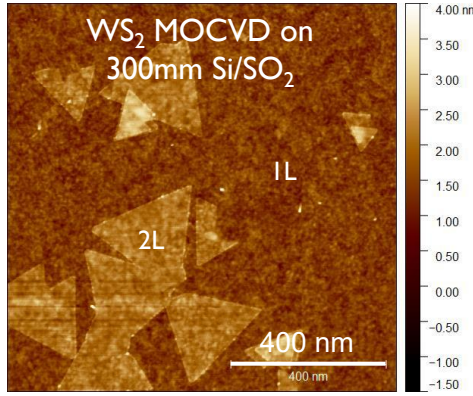
High yield for baseline flow & direct dep WS_2

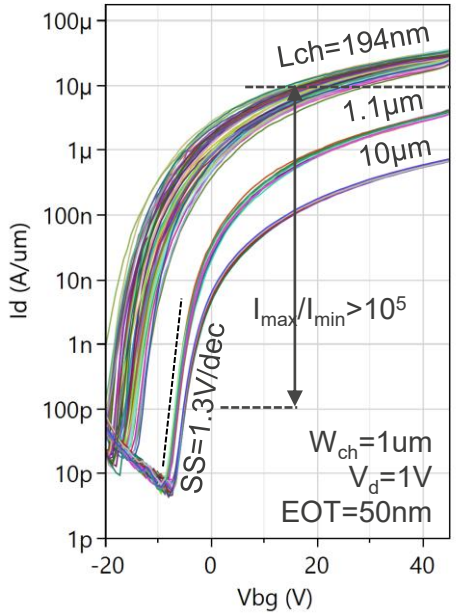
Previous maskset
Yield=91% (307/336)

Improved maskset
Yield>99% (133/133)



T. Schram et al., VLSI 2021





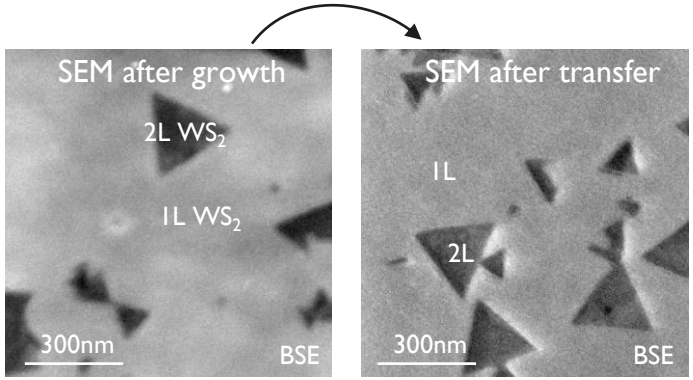
- Yield>99% with current maskset
- Yield defined as $I_{max}/I_{min}>10^5$

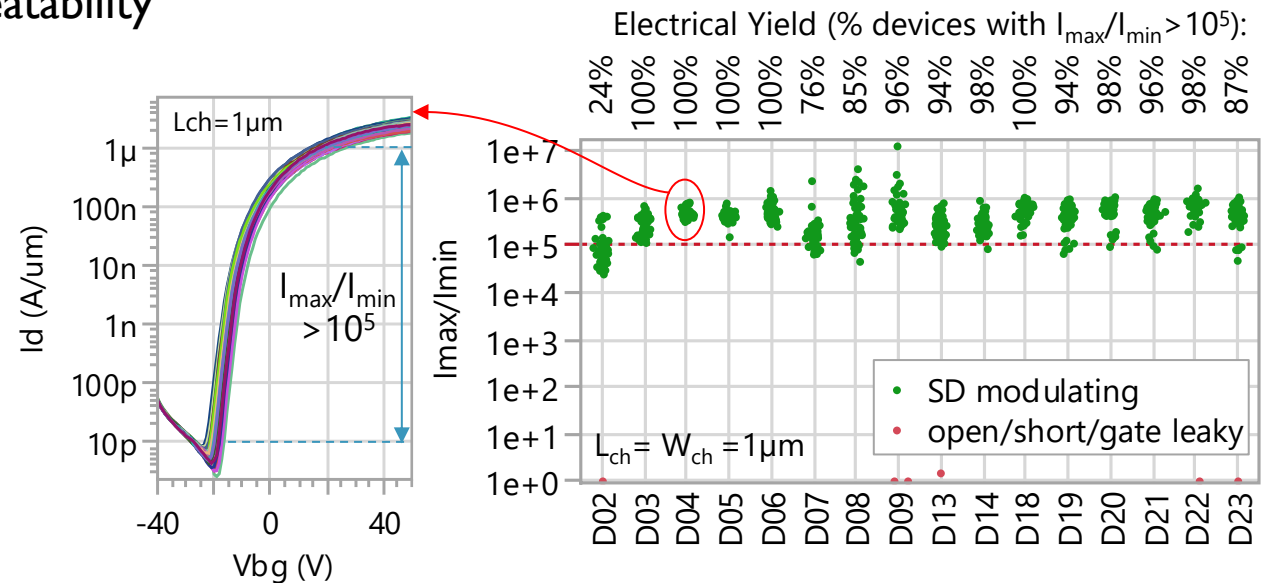
TLM analysis
- WS_2 µ=3 cm^2/Vs
- Ti side contact
  R_c = 5-50kΩµm at n=$10^{13}cm^{-2}$

T. Schram & Q. Smets et al. (imec), *Discov Electron* **3**, 15 (2026) doi:10.1007/s44291-026-00164-4

High yield for 300 mm transferred WS_2

- Transfer WS_2 to "fresh" device wafers
- Yield >95% for most wafers
- Good wafer-to-wafer repeatability

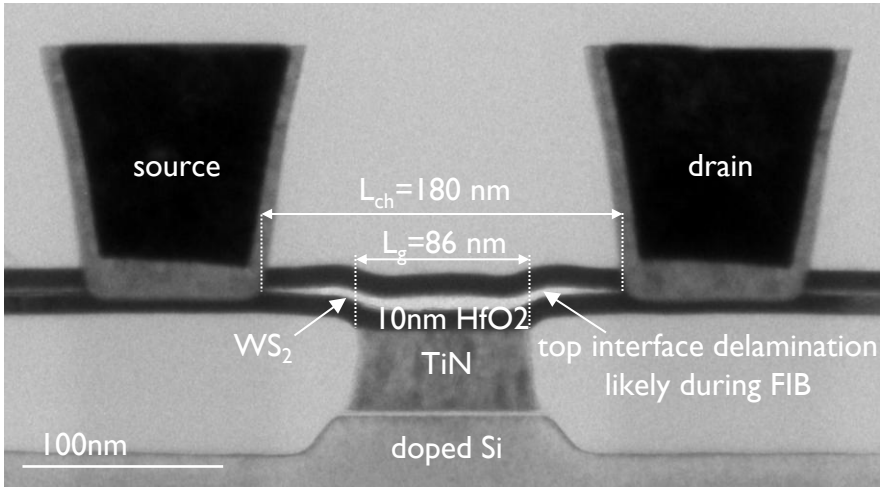


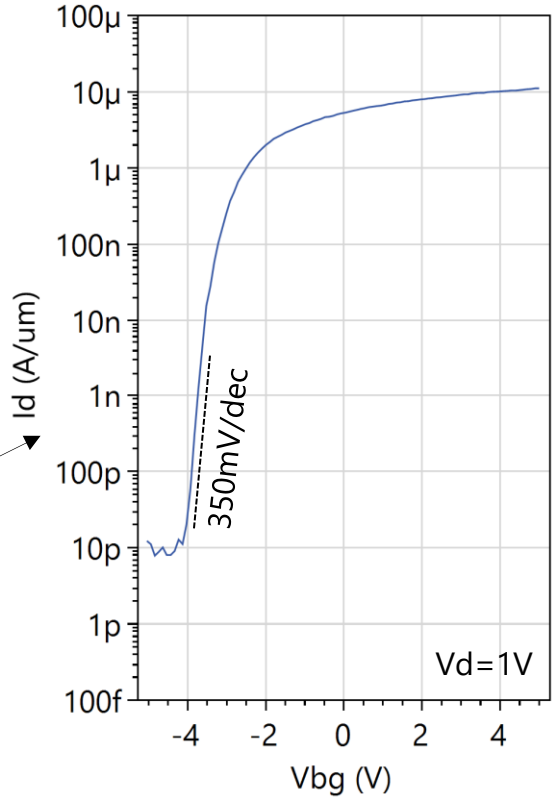


S. Ghosh et al.(imec), *VLSI* (2024) doi:10.1109/VLSITechnologyandCir46783.2024.10631364

Back EOT scaling enabled by WS_2 transfer to high-k

- 300mm transfer of WS_2 to local back gates with high-k dielectric
- g_m & SS improvement with EOT scaling
- Substrate flexibility with transfer route

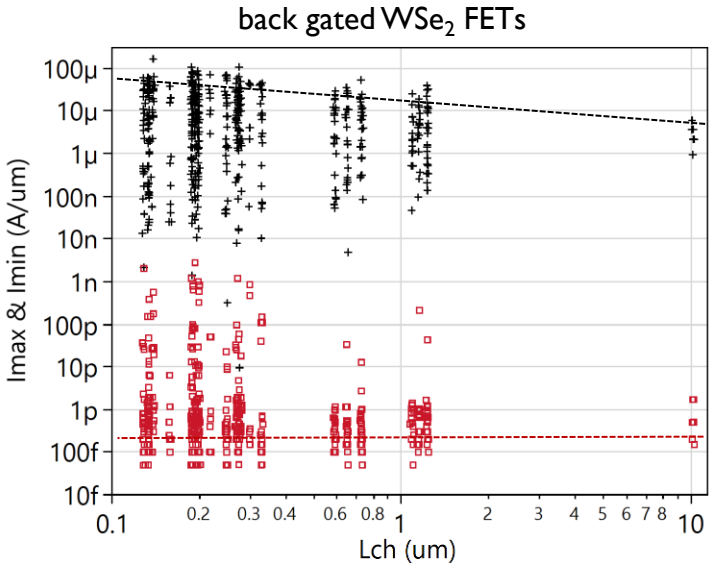


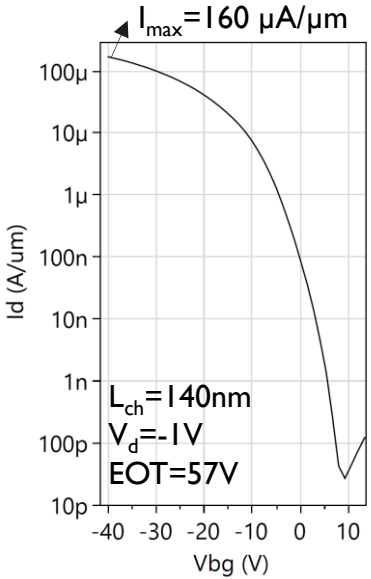


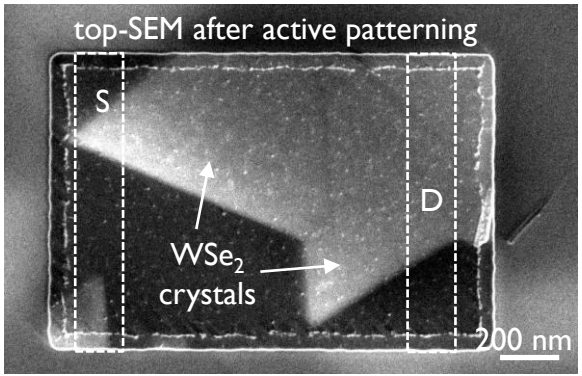
S. Ghosh et al.(imec), *VLSI* (2024) doi:10.1109/VLSITechnologyandCir46783.2024.10631364

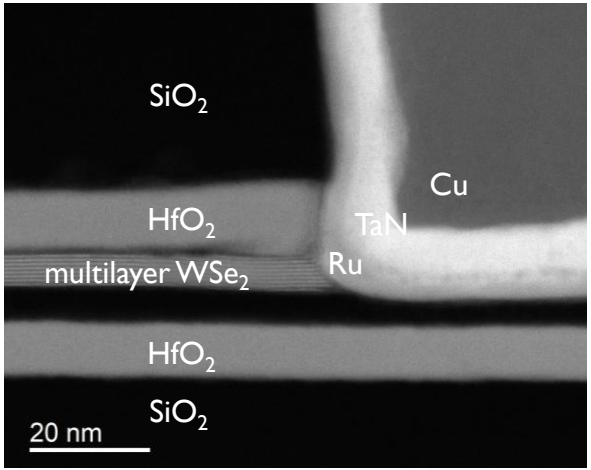
pFETs with WSe2 by MOCVD on 300mm Si/SiO_2

- WSe_2 MOCVD direct growth
- Side contacts with Ru (CVD)
- Variability due to non-closed WSe_2
- WSe_2 mobility reaching over 30 cm^2/Vs.





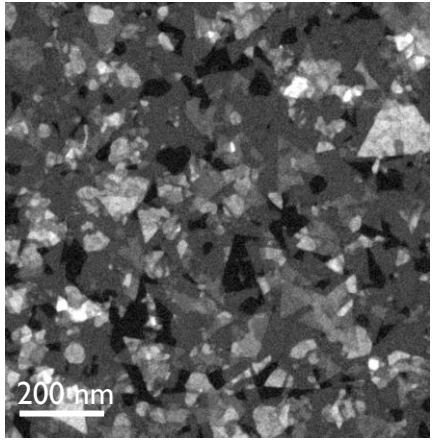


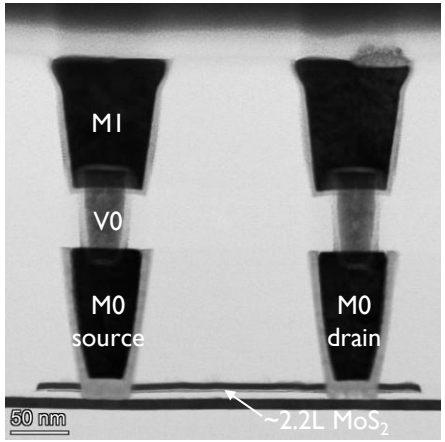


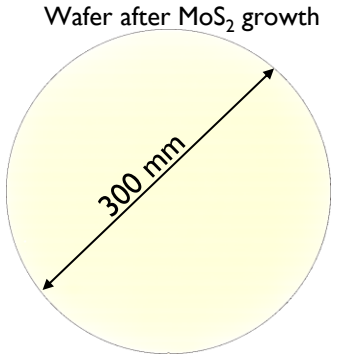
nFETs with MoS_2 by MOCVD on 300mm Si/SiO_2

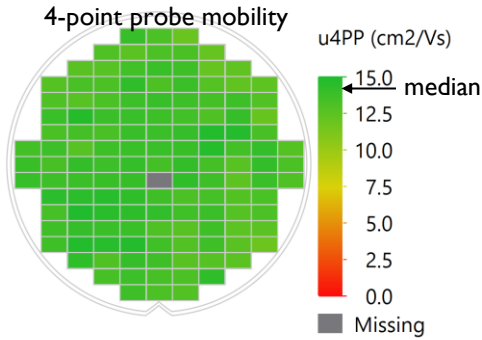
- Aixtron/imec collaboration on tool & process development
- MOCVD at moderate T=600 °C yields ~2.2ML MoS_2 (average)
- Good wafer-level uniformity, median mobility of 14 cm^2/Vs











Side contacts are reliable, but have limitations

Benefits

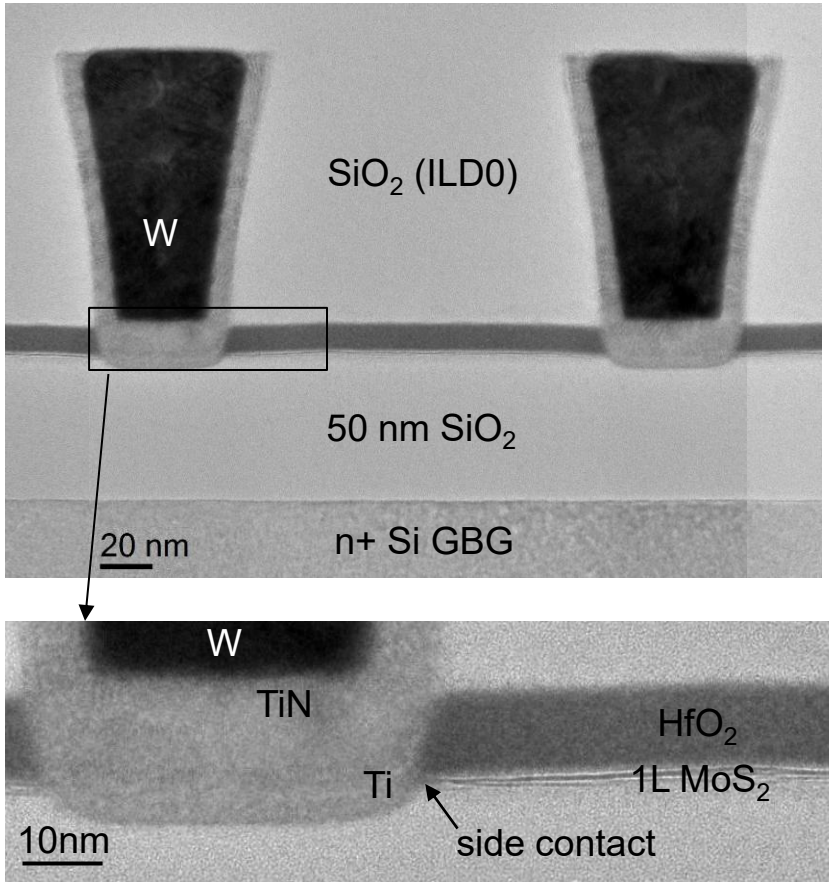
- Reliable (timed etch)
- Anchoring

Drawbacks

- No global back gate scaling
- Poor control of exposed TMDC edge, small contact area, poor R_c

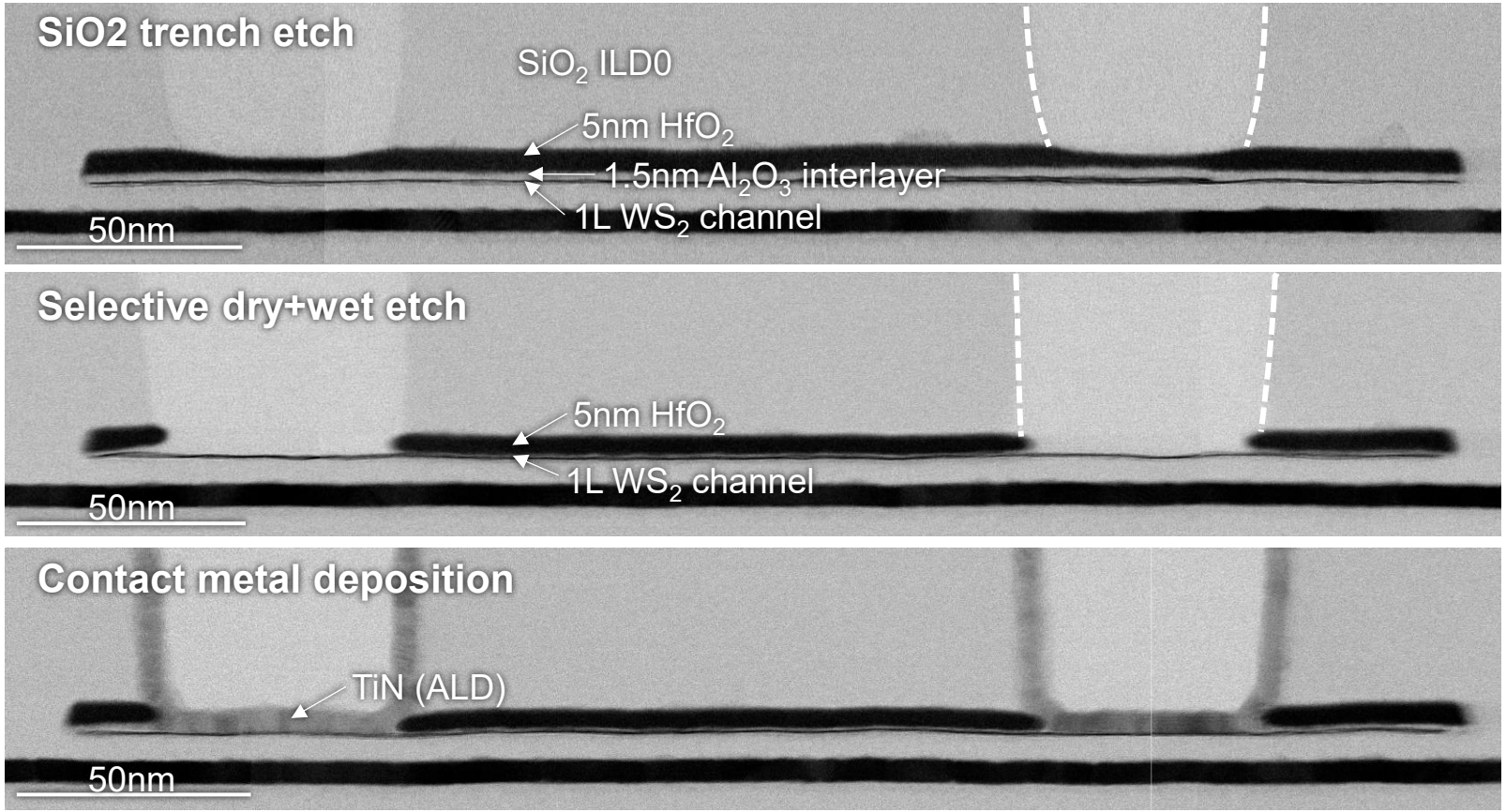
type	Channel	Contact	Rc(Ω-µm)
imec fab	1L SG WS_2	Ti side	50 k
		TiN side	125 k
	1L LG MoS_2	Ti side	2.5 k
	multilayer WSe_2	Ru side	5.8 k

→ Develop top contact module in fab



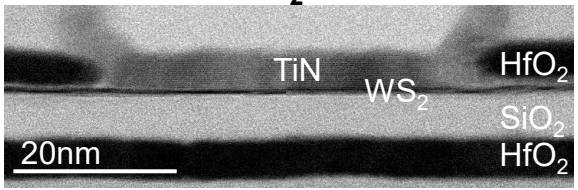
T. Schram & Q. Smets et al. (imec), *Discov Electron* **3**, 15 (2026) doi:10.1007/s44291-026-00164-4

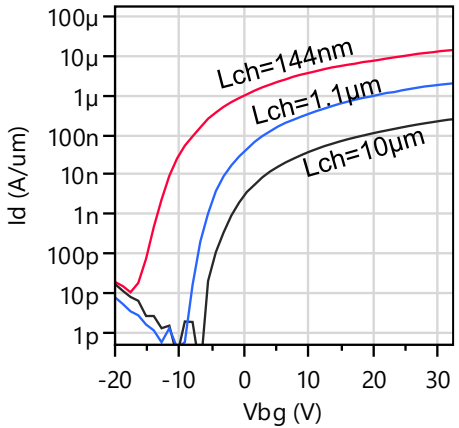
Dielectric etch process highly selective to 2D



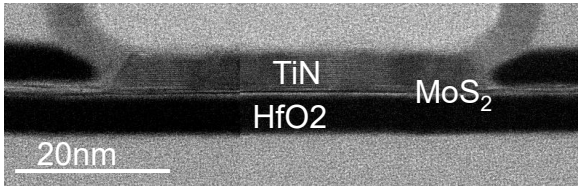
Top contacts to WS_2, MoS_2, WSe_2

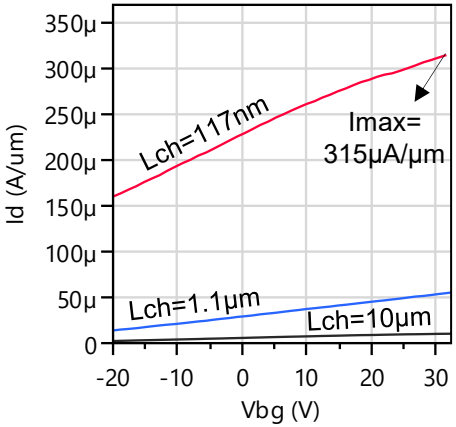
WS_2 / TiN



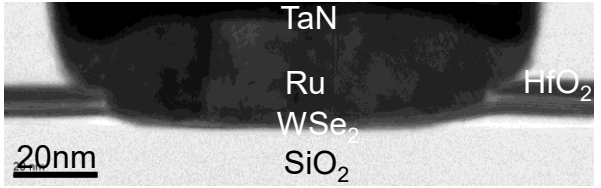


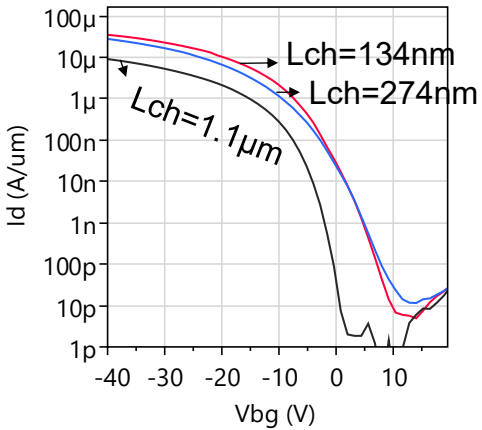
MoS_2/TiN





WSe_2/ Ru





- Operational top contacts for WS_2, MoS_2, WSe_2
- Epitaxial relationship between MoS_2, WS_2 and TiN ALD
- WS2 pFETs integrated with Ru top contacts

Q. Smets & T. Schram et al., *IEDM* (2025) doi:10.1109/IEDM50572.2025.11353796

Benchmarking contact resistances fab & lab

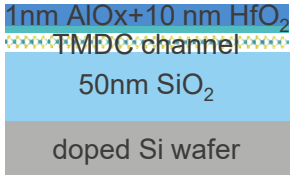
type	Channel	Contact	Rc(Ω-µm)	Method
imec fab [1]	1L SG WS_2	Ti side	50 k	best Rtot
		TiN side	125 k	best Rtot
		TiN top	50 k	best Rtot
	1L LG MoS_2	Ti side	2.5 k	best Rtot
		TiN top	1.6 k	best Rtot, n_s=5E13 cm^{-2}
	multilayer WSe_2	Ru side	5.8 k	TLM, n_s=1E13 cm^{-2}
		Ru top	9 k	TLM, n_s=1.3E13 cm^{-2}
imec lab [2-3]	1-2L MoS_2 [2]	Ni/Pd liftoff	440	best Rtot
	2L WSe_2 [3]	Pd liftoff	700	TLM, n_s=2E13 cm^{-2}
literature lab [4-7]	3L MoS_2	Y	69	TLM [4]
	1L MoS_2	Sb liftoff	42	TLM, n_s=3E13 cm^{-2} [5]
	1L MoS_2	Bi liftoff	123	TLM, n_s=1.5E13 cm^{-2} [6]
	1L WSe_2	Pt liftoff	616	TLM, n_s=1E13 cm^{-2} [7]
Requirement HP	-	-	<100	

Material & process improvements still needed

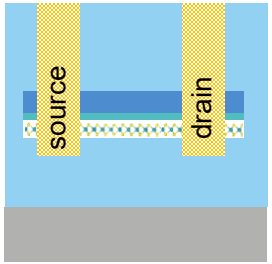
[1] Q. Smets et al., IEDM 2025 (imec)
[2] F. Xi et al., IEDM 2024 (imec)
[3] T. D. Ngo et al., IEDM 2025 (imec)
[4] J. Jiang et al., Nature Elec. (Peking univ.)
[5] W. Li et al., Nature 2023 (Nanjing)
[6] P.C. Shen et al., Nature 2021 (MIT)
[7]A. Qiu et al., IEDM 2025 (Peking univ.)

Imec 300 mm integration flow for TMDC FETs (with top gate)

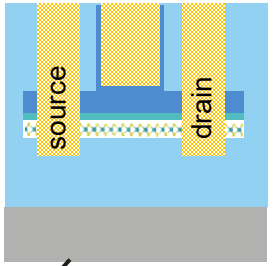
- 300 mm Si wafer
- back gate stack dep.
- TMDC dep./transfer
- Al_2O_3 IL (TMA soak)
- HfO_2 cap (ALD)



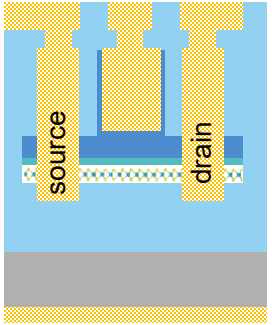
- Active patterning
- SiO_2 encaps. & CMP
- M0 side contacts



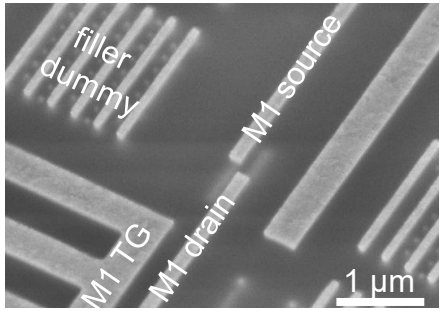
- TG trench etch
- HfO_2 top-up
- TiN/W fill
- CMP

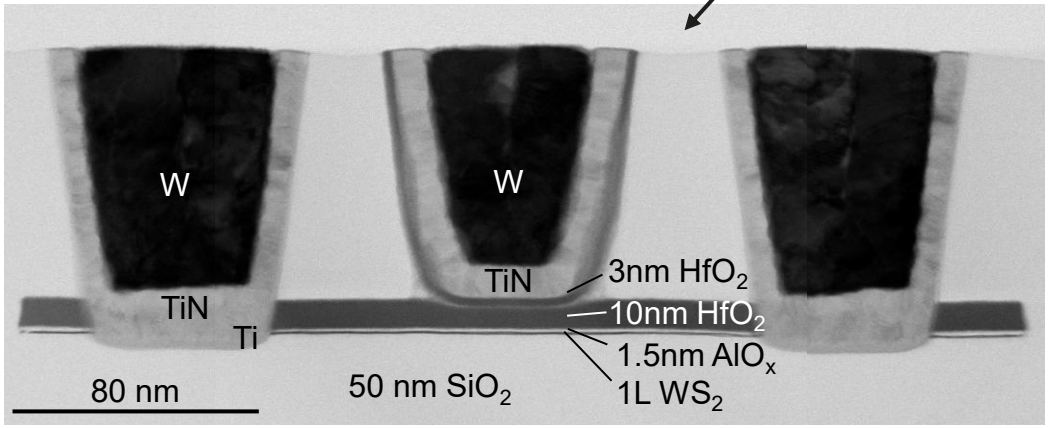


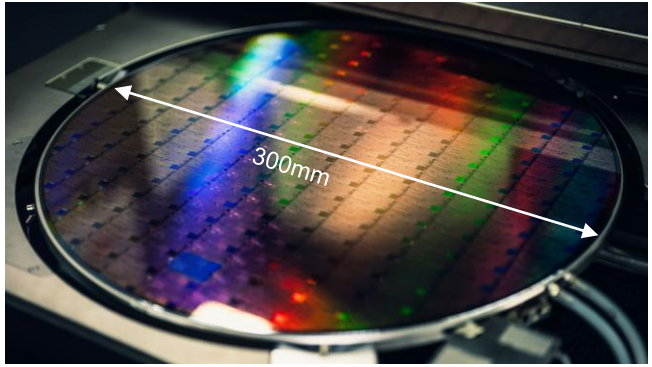
- V0 damascene
- M1 damascene
- backside metal



Top view:



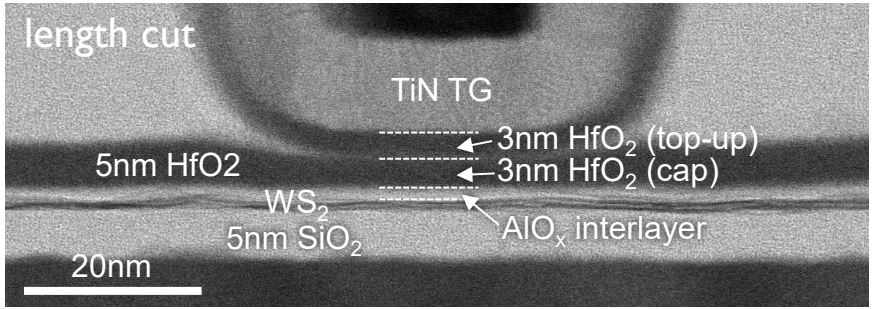


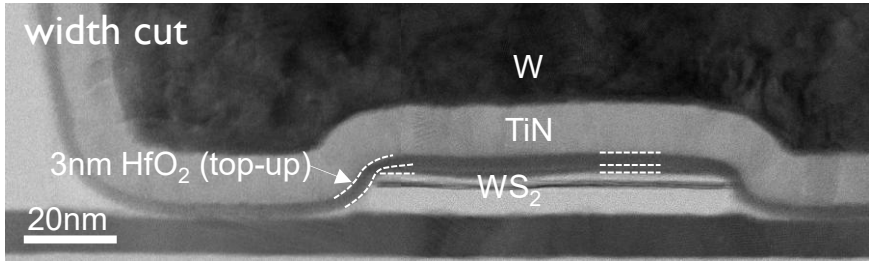


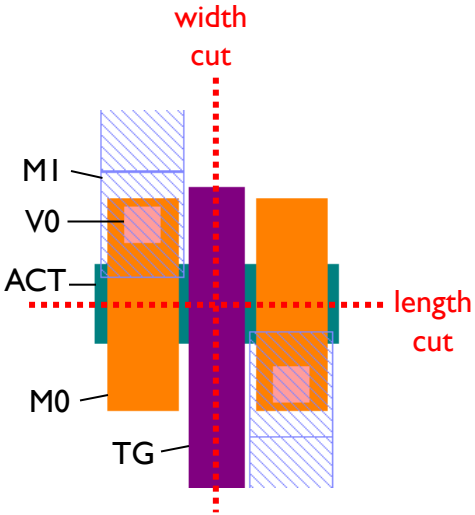
T. Schram & Q. Smets et al. (imec), *Discov Electron* **3**, 15 (2026) doi:10.1007/s44291-026-00164-4

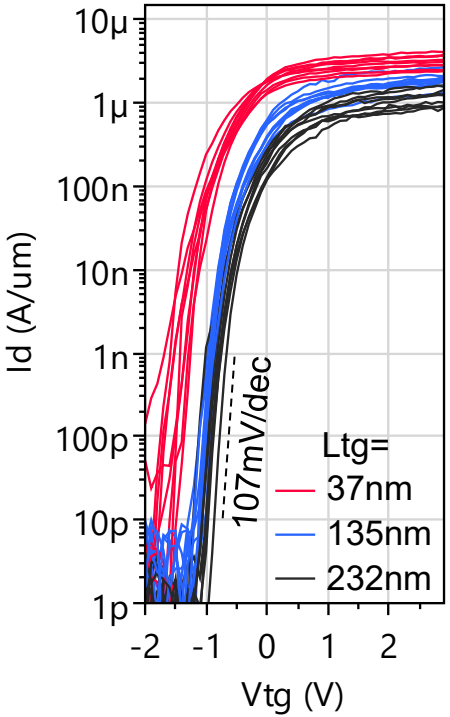
WS_2 baseline TG stack needs 3 dielectric layers

- Goal: assess and develop gate stack
- 3 dielectric layers required by dielectric-first flow
- median SS=107mV/dec





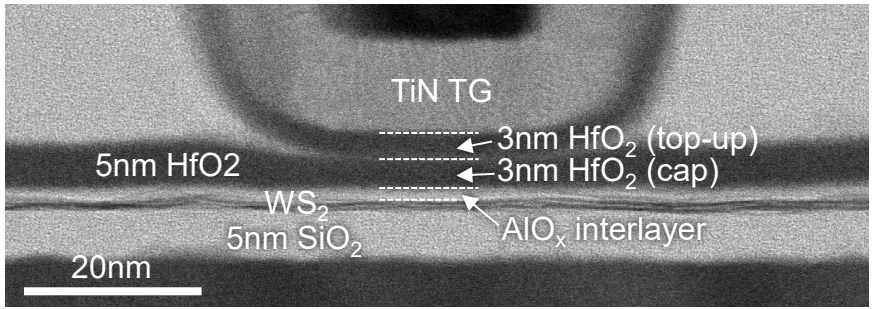


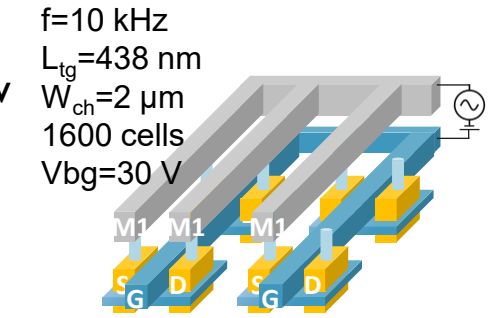


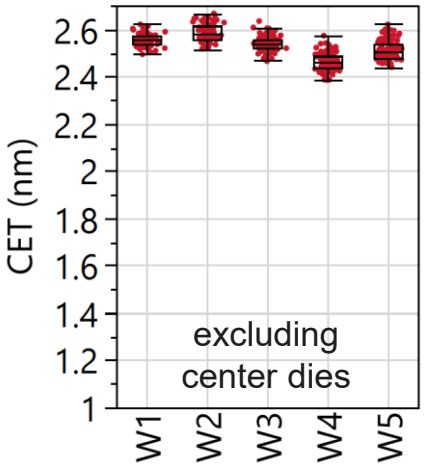
Q. Smets & T. Schram et al., *IEDM* (2025) doi:10.1109/IEDM50572.2025.11353796

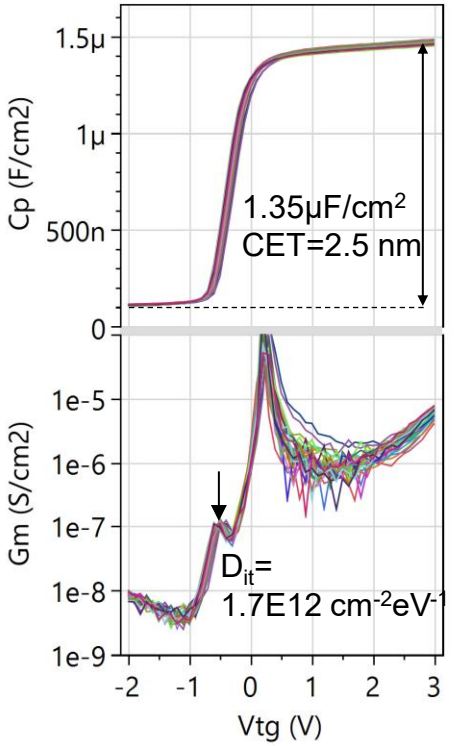
WS_2 baseline TG has stack good reproducibility from C-V

- Goal: assess and develop gate stack
- 3 dielectric layers required by dielectric-first flow
- FETCAP test structures
  - CET=2.5nm
  - midgap D_{it}=1.7x10^{12} cm^{-2}eV^{-1}





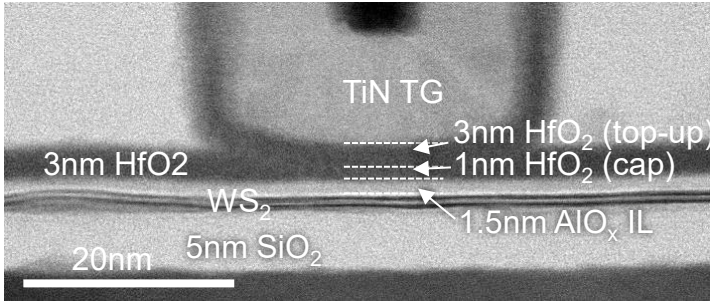




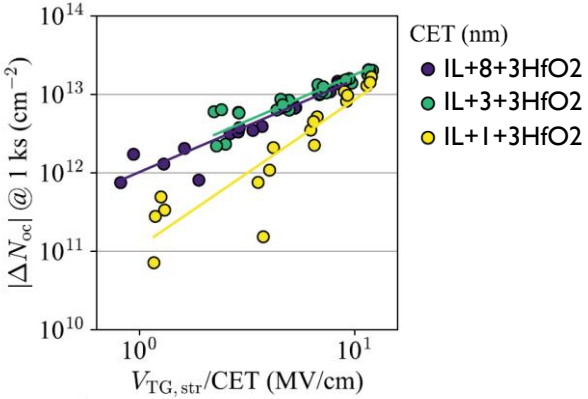
Q. Smets & T. Schram et al., *IEDM* (2025) doi:10.1109/IEDM50572.2025.11353796

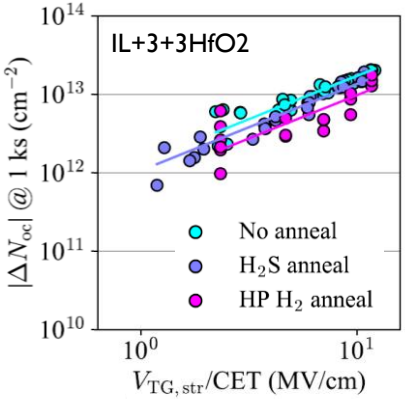
Gate stack reliability & improvement strategies

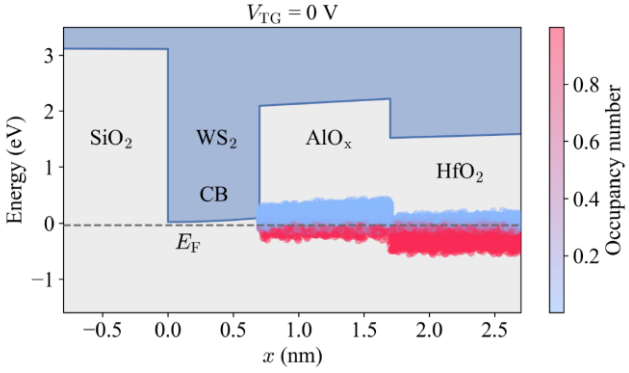
- Reliability improvement by bulk HfO_2 scaling

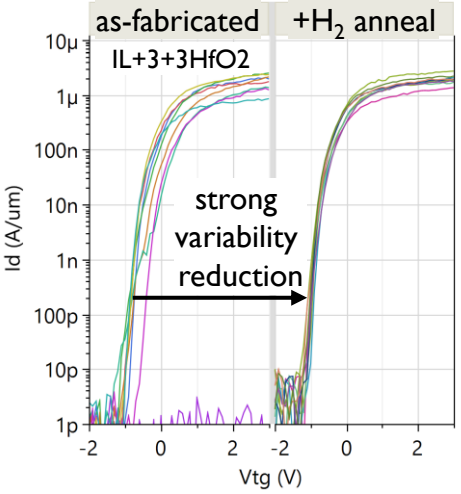


- High-pressure hydrogen anneal 250°C 20bar (HPSP)
  - minor reliability improvement
  - strong variability reduction
- More effective: band alignment engineering





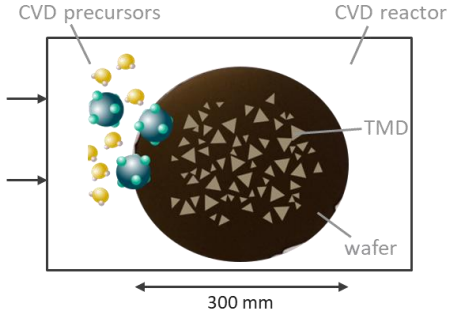




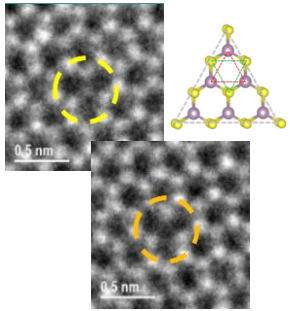
L. Panarella et al., *EDTM* (2026) doi:10.1109/EDTM65772.2026.11497294

Key challenges to tackle in the coming years

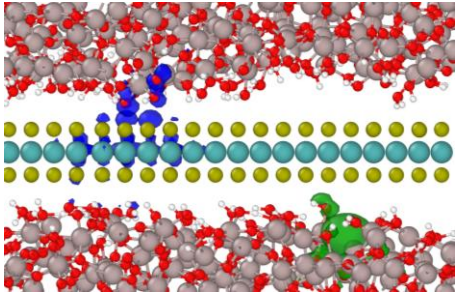
Manufacturable 2D growth chemistry



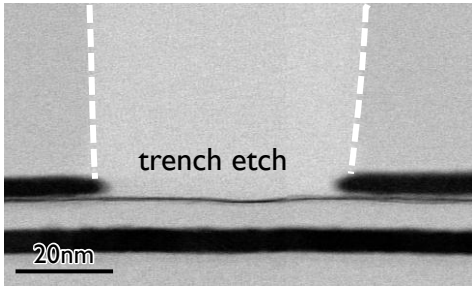
Post-transfer defect passivation



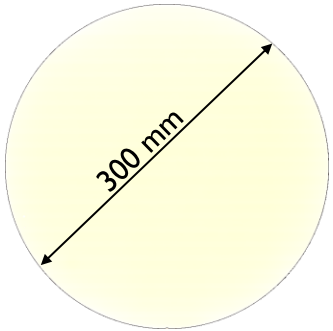
Dielectric-induced band edge fluctuations



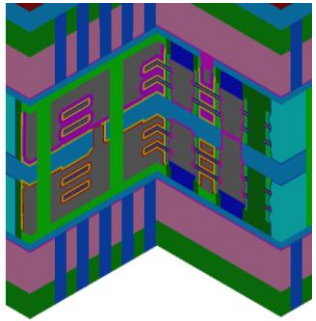
selective etch & clean



300mm growth for pMOS



2D-tailored standard cell



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Gautam Gaddemane
Gouri Sankar Kar
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