2D PILOT LINE

Graphene Integration on SiN Integrated Photonics Platform

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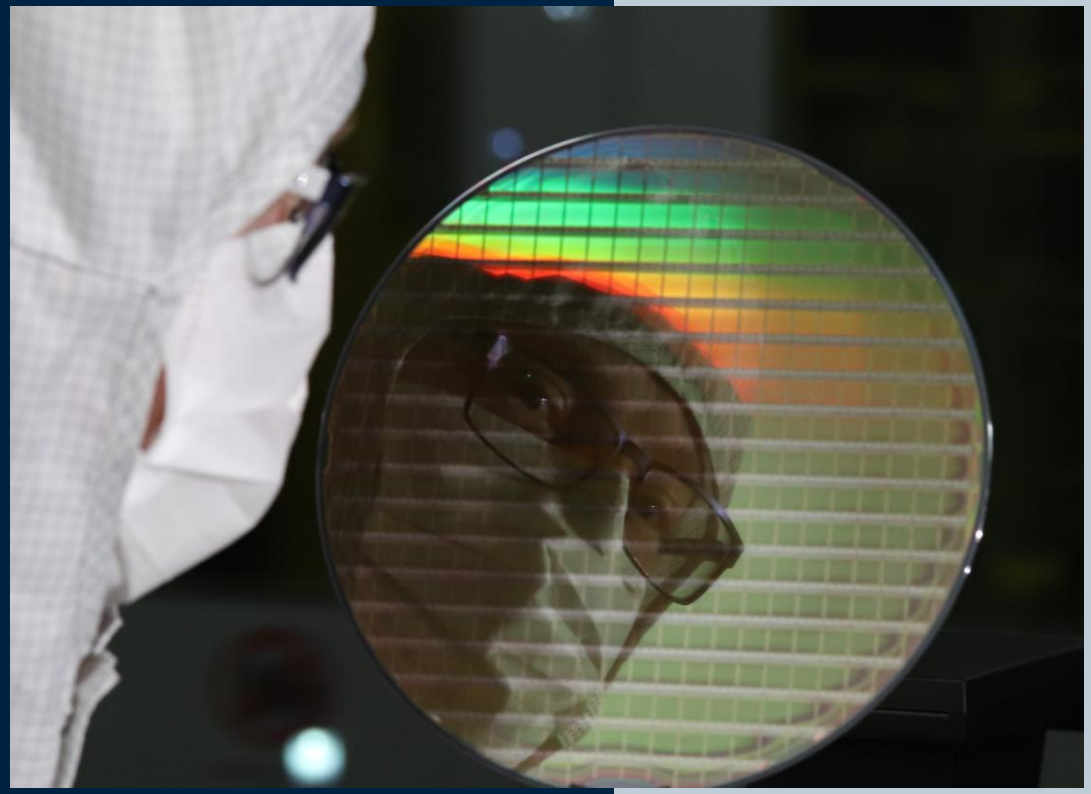
GRAPHENE FLAGSHIP

VTT

Funded by the European Union

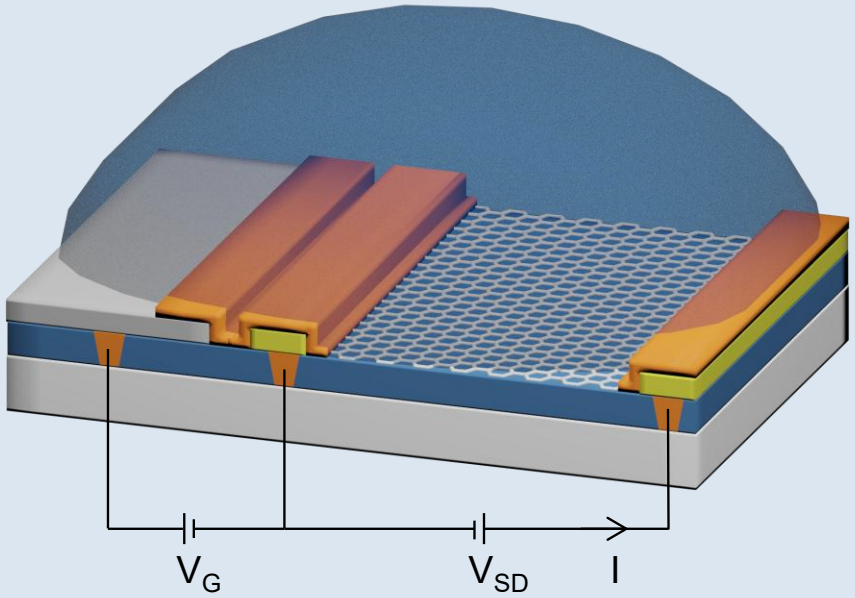
Outline

- 2D Material Development at VTT
- VTT Integrated Photonics
- Graphene Modulator Integration
- Graphene Processing Building Blocks
- Process Design Kit
- Summary

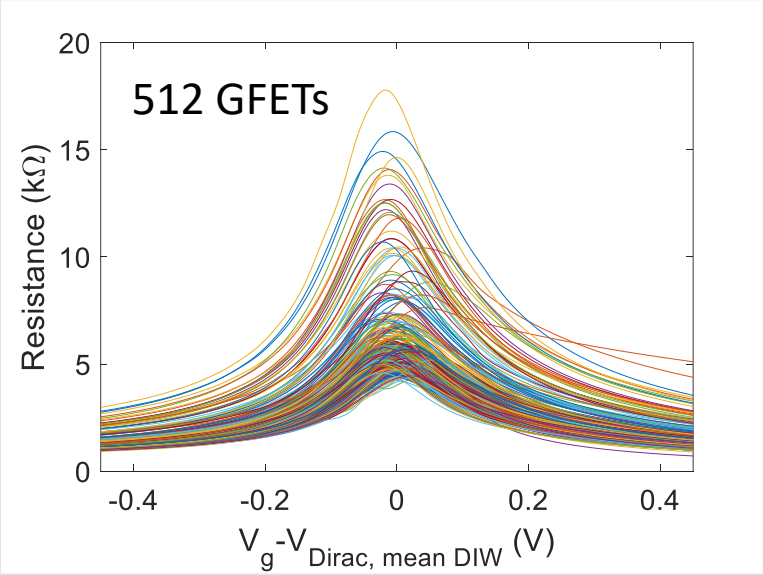


2D Material Development at VTT

- 200 mm wafer scale processing
- Focused on post CMOS BEOL integration and integrated photonics

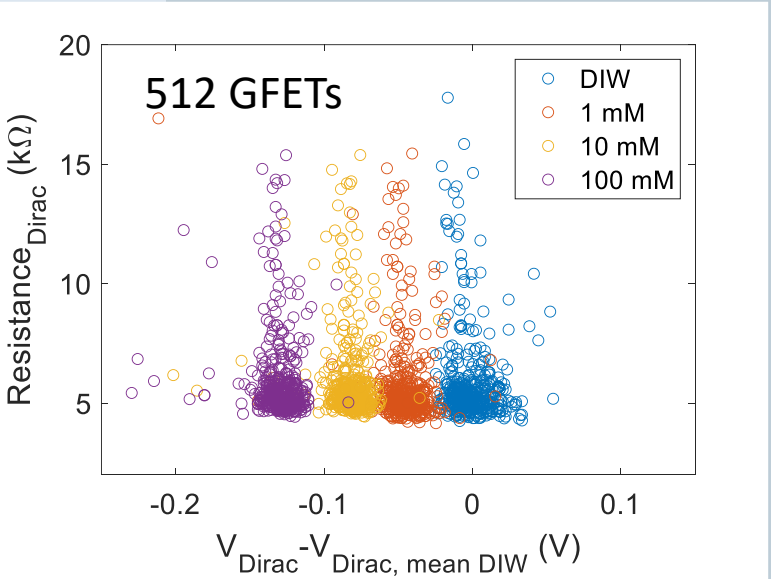


Gating via the liquid



Proof-of-concept demonstrated!

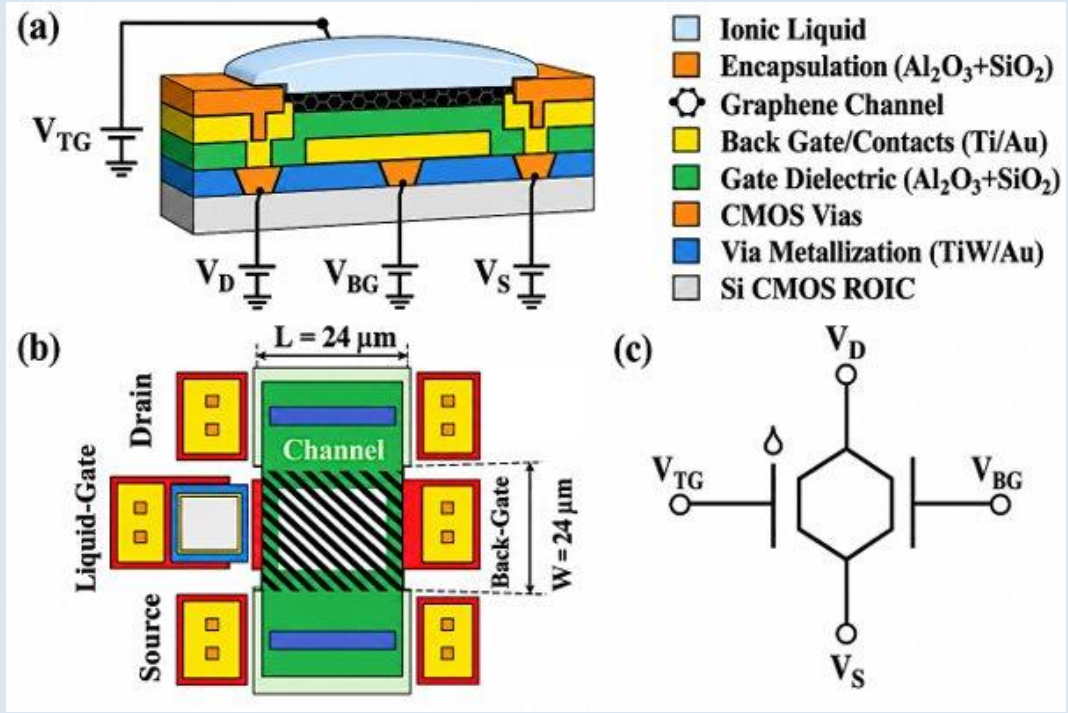
NaCl concentration series



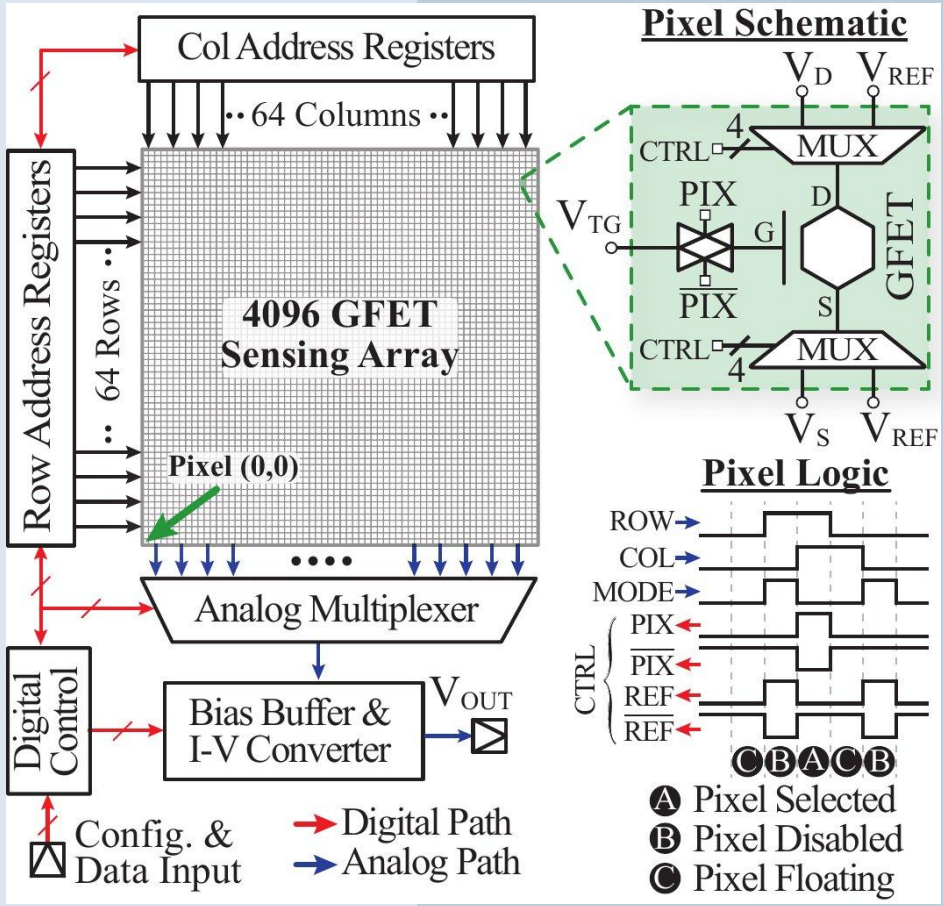
Soikkeli, Miika, et al. "Wafer-scale graphene field-effect transistor biosensor arrays with monolithic CMOS readout." *ACS Applied Electronic Materials* 5.9 (2023): 4925-4932.

2D Material Development at VTT

- Graphene sensor post-CMOS integration PDK built by Cadence
  - The PDK includes DRC, LVS and device model.



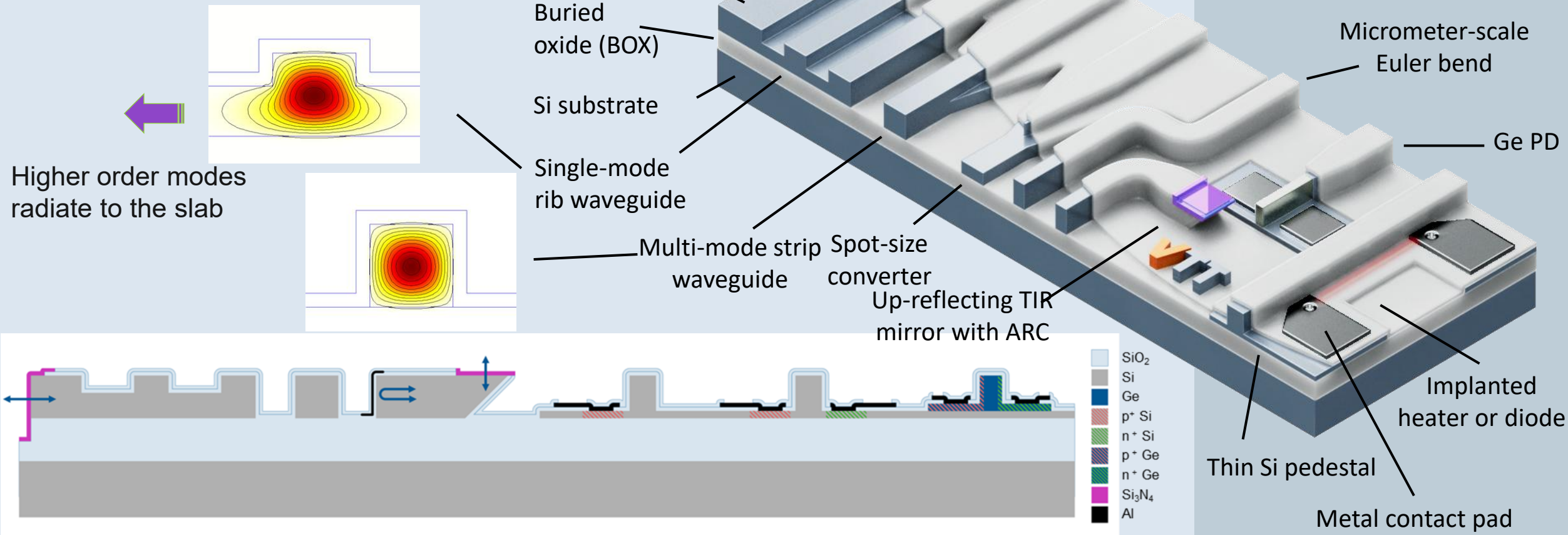
Numan, Omar, et al. "Compact Modeling and Device–Circuit Co-Simulation of Post-Processed GFET–CMOS Sensor Systems ." *ESSERC 2026*.



VTT Integrated Photonics

Thick SOI Platform

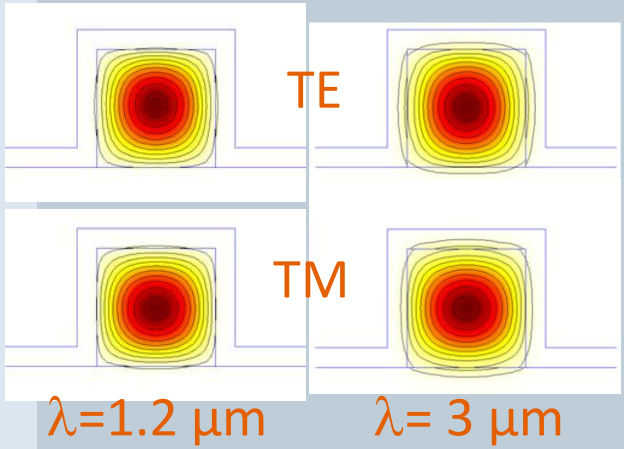
Passive and active photonic integrated circuits (PICs) in 3 µm thick silicon-on-insulator (SOI)

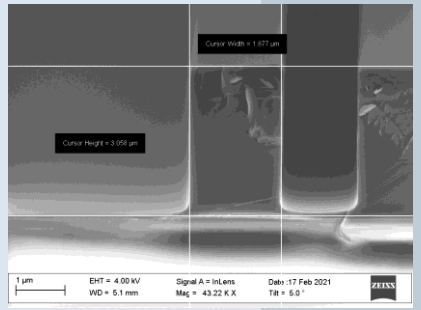


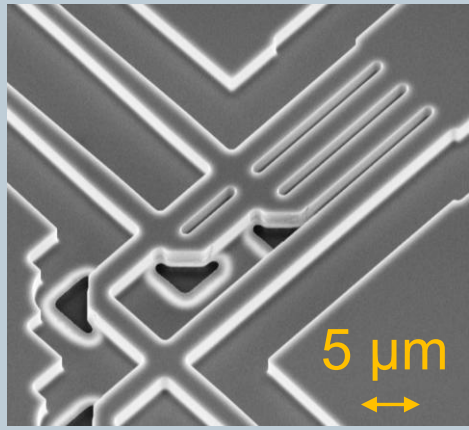
Aalto, Timo, et al. "Photonic Integrated Circuit Platform on 3 µm Thick Silicon-on-Insulator and Its Application Examples." *Nanophotonics* 15.17 (2026): e70271.

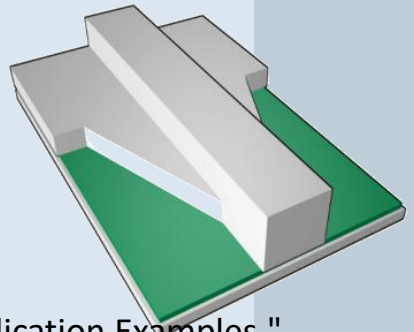
Unique aspects of micron-size SOI waveguides

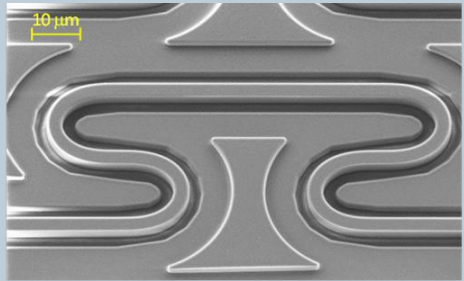
1. Combination of SM rib and MM strip waveguides
   - Keeping light in the fundamental mode
   - Effectively single-moded waveguide circuits
2. Large core allows to propagate high power (>1 W)
   - Limited by two-photon absorption at $\lambda < 2.4$ µm
3. Ultra-high mode confinement
   - Reduced sensitivity to fabrication tolerances
   - Zero birefringence in (square) strip waveguides
   - Small 0.02 - 0.15 dB/cm loss for both waveguides
   - Ultra-wide wavelength range (1.2 - 6 µm)
   - Ultra-dense integration with strip waveguides







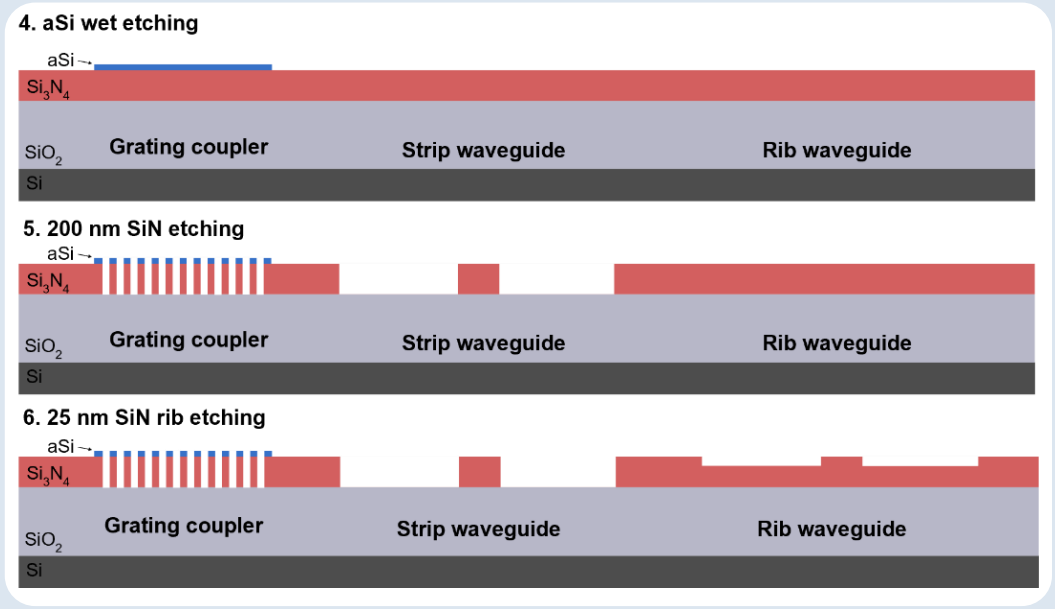




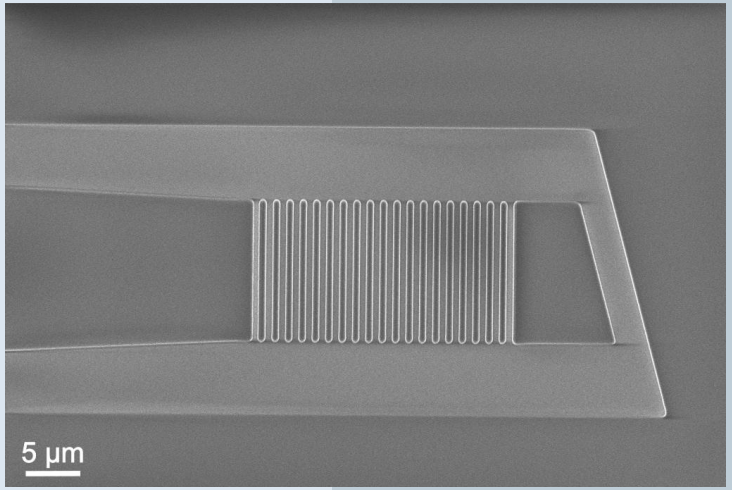
Aalto, Timo, et al. "Photonic Integrated Circuit Platform on 3 µm Thick Silicon-on-Insulator and Its Application Examples." *Nanophotonics* 15.17 (2026): e70271.

VTT Integrated Photonics
SiN Platform

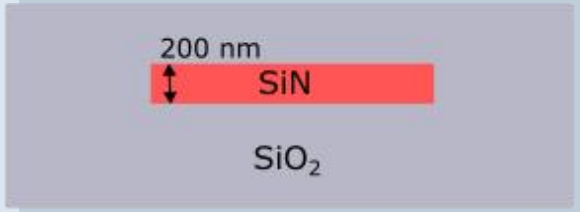
- SiN platform includes strip and rib waveguides.
- The process can be fabricated with i-line lithography
- The platform is designed for wide spectral bandwidth
  - Passives tested and verified at 900 nm, 1310 nm and 1550 nm.

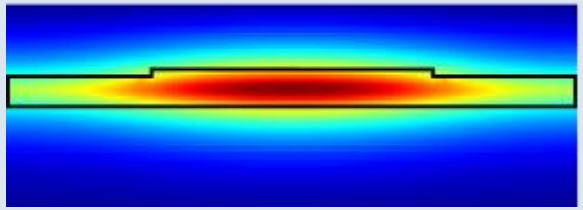


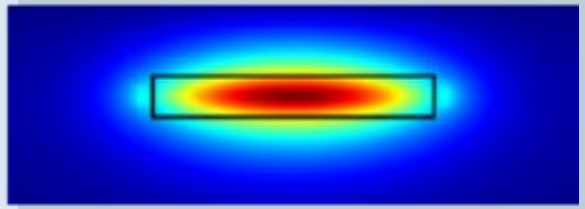
Insertion losses of ~5.3 dB per coupler





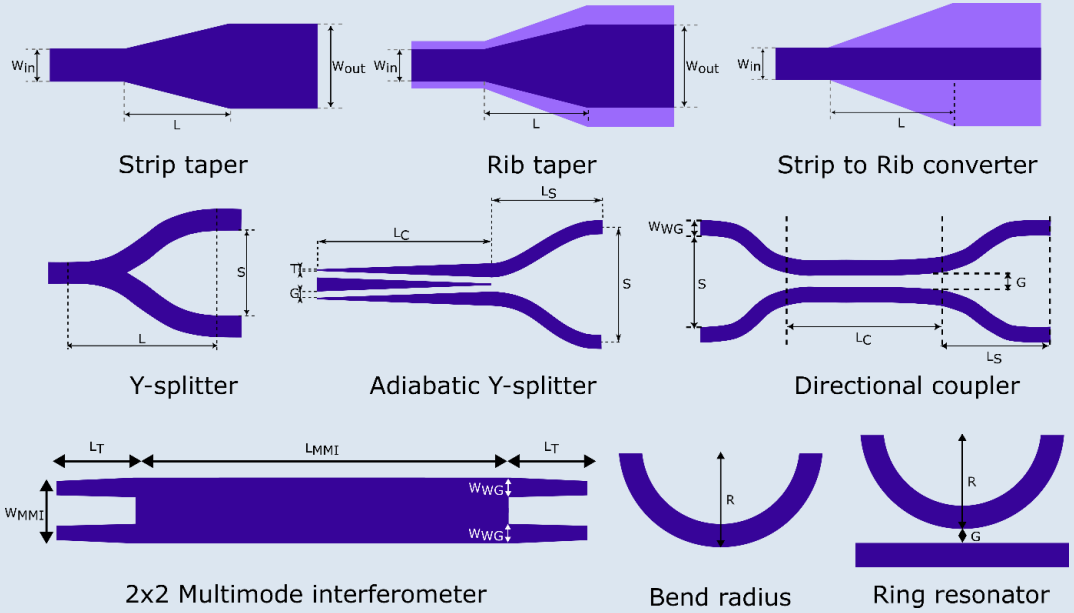


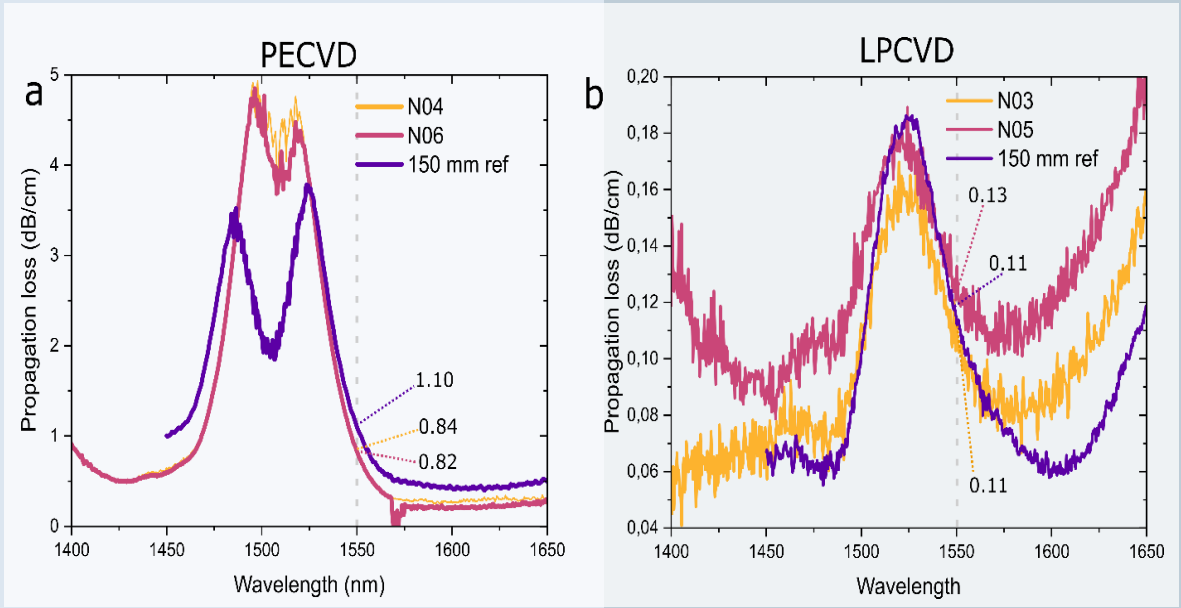




VTT Integrated Photonics
SiN Platform

- The platform includes simulated and verified passives components to enable PIC design at 900 nm, 1310 nm and 1550 nm.
- Low temperature (PECVD) and high temperature (LPCVD) processes
- Propagation losses below 1 dB/cm at 1550 nm

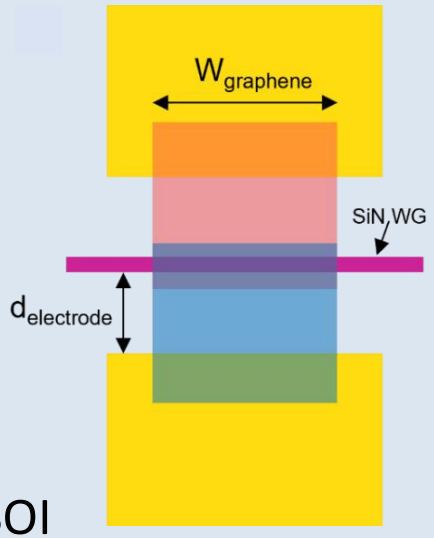


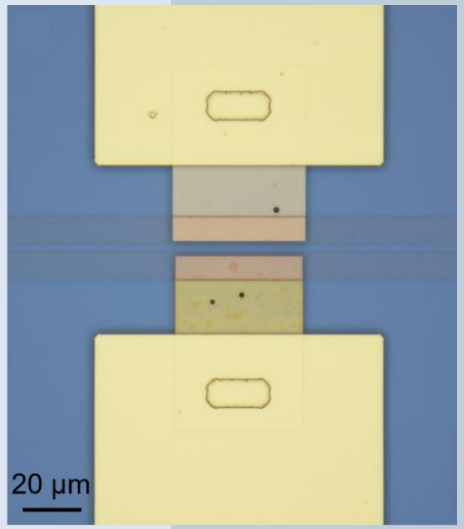


Graphene Modulator Integration

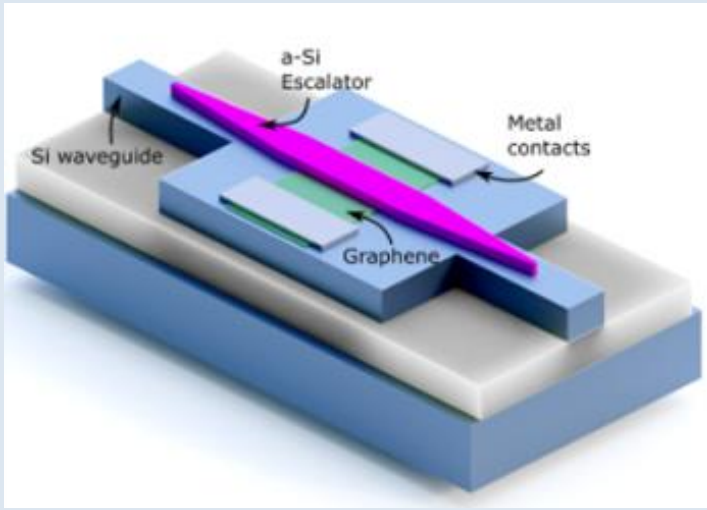
- Graphene in integrated Photonics
  - Broadband optical response
  - High carrier mobility
  - Heterogeneous integration
  - Electrically tunable absorption

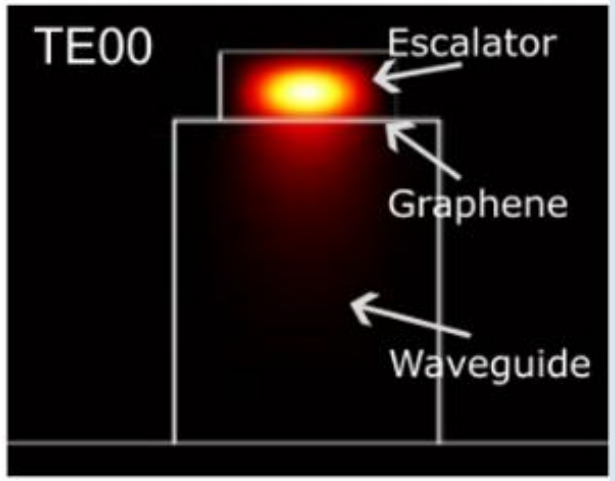
Modulator integrated on SiN

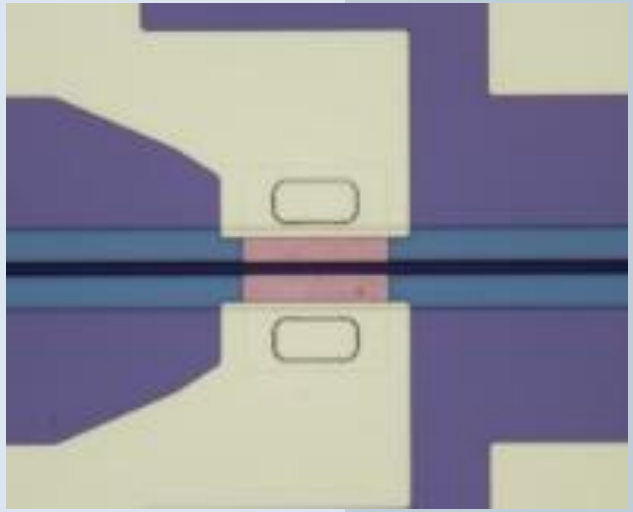




Graphene detector integration on thick SOI

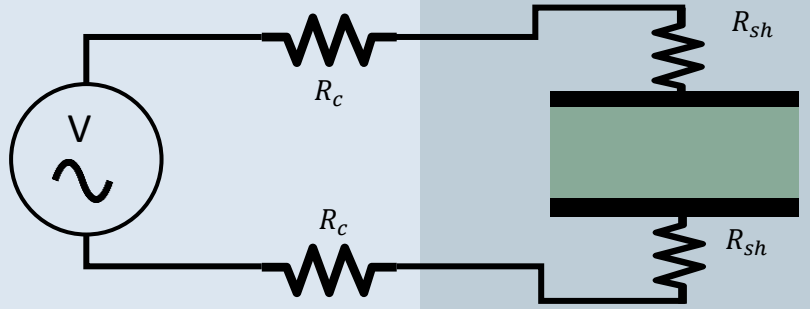


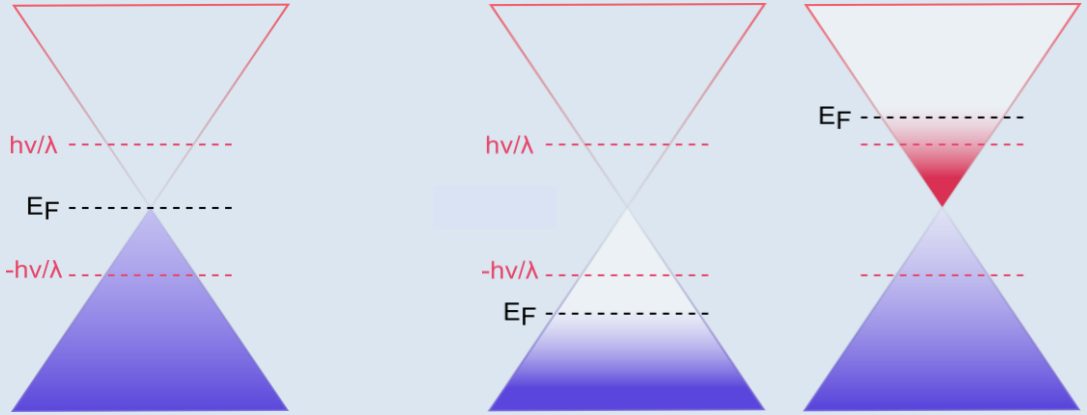




Graphene Modulator Integration

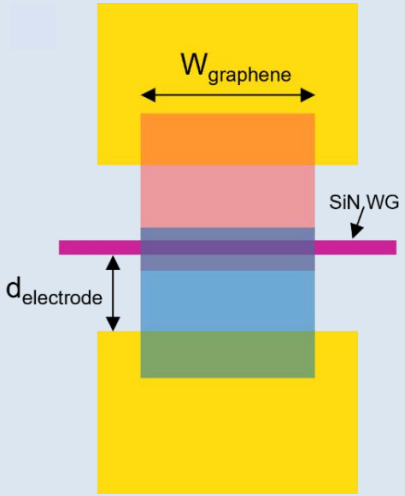
- Modulator are included to our SiN platform
- Electro-absorption modulators composed of a double-graphene layer structure with Al_2O_3 dielectric.
- Three dielectric thickness options – 10 nm, 20 nm and 30 nm

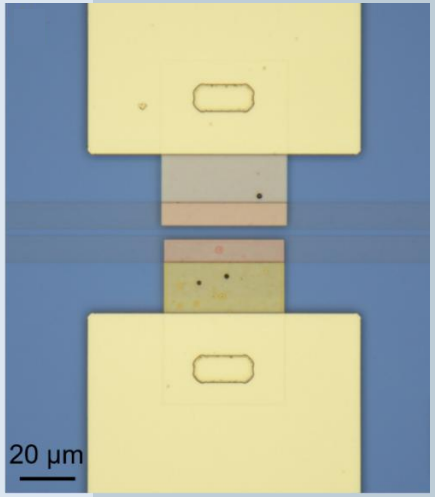




Absorption!

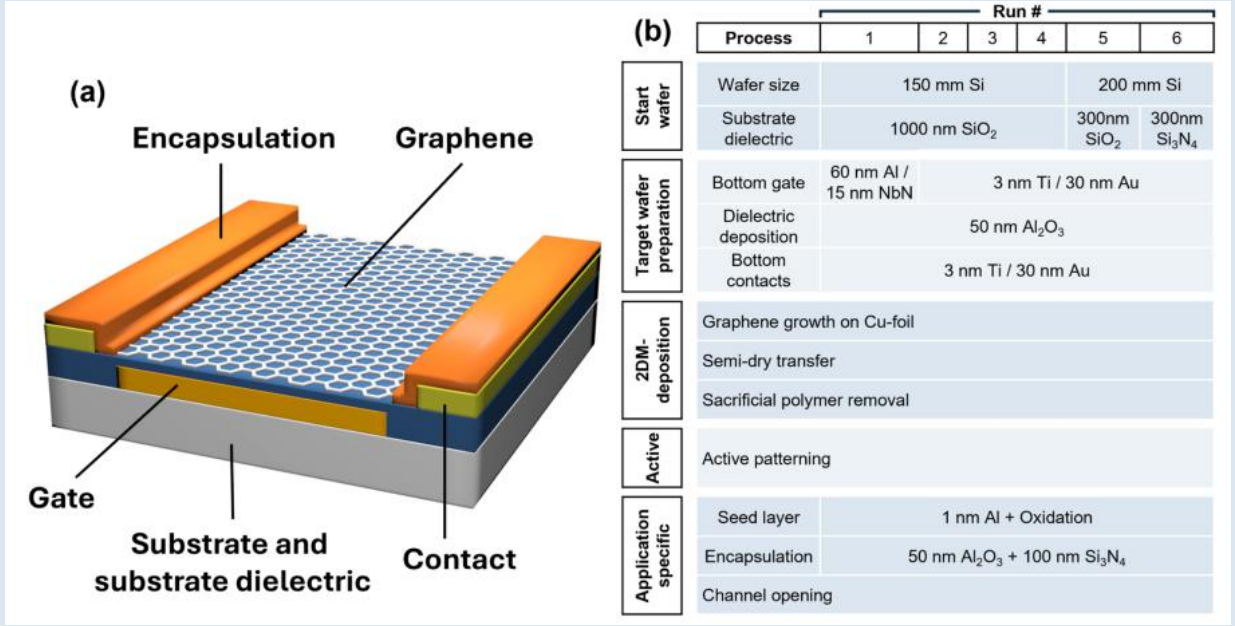
No Absorption!
Pauli blocking





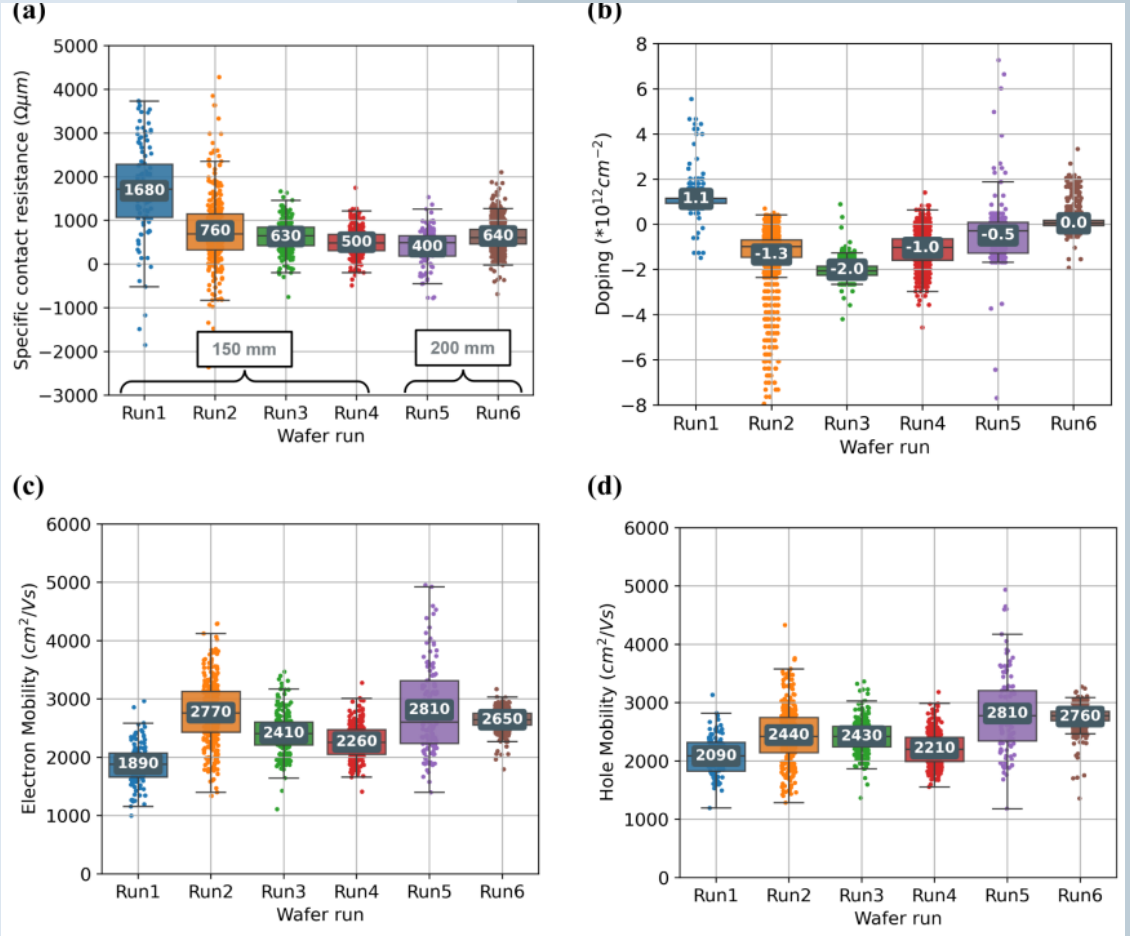
Graphene Process Modules

- 200 mm wafer-scale processing
- Ohmic contacts
- Low residual lithography
- Encapsulation module



(b)

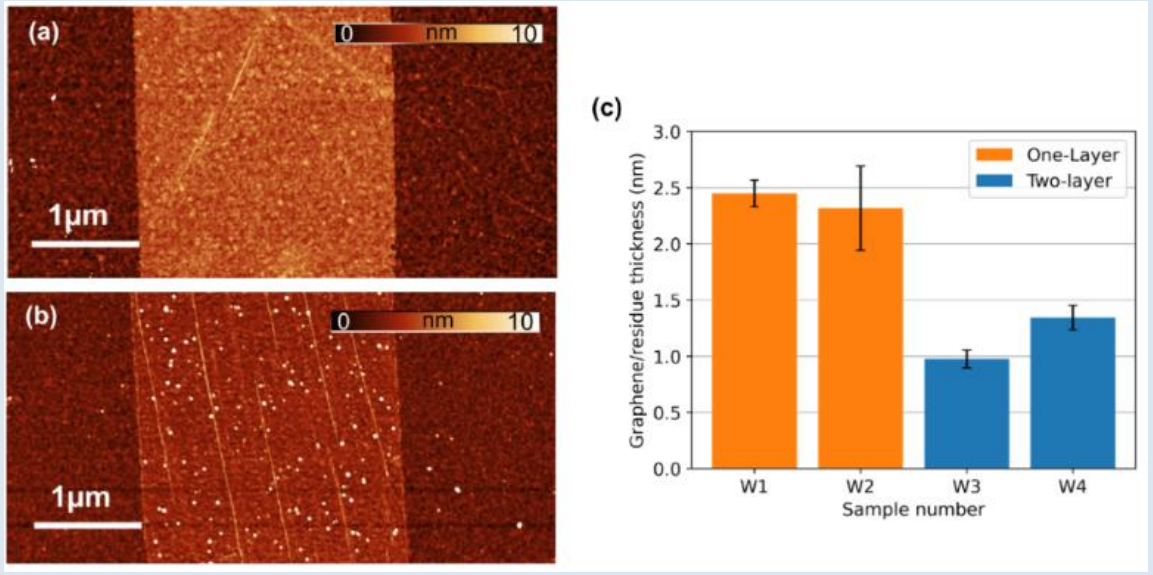
	Process	Run # 1	2	3	4	5	6
Start wafer	Wafer size	150 mm Si				200 mm Si	
	Substrate dielectric	1000 nm SiO_2				300nm SiO_2	300nm Si_3N_4
Target wafer preparation	Bottom gate	60 nm Al / 15 nm NbN	3 nm Ti / 30 nm Au				
	Dielectric deposition	50 nm Al_2O_3					
	Bottom contacts	3 nm Ti / 30 nm Au					
2DM-deposition	Graphene growth on Cu-foil						
	Semi-dry transfer						
	Sacrificial polymer removal						
Active	Active patterning						
Application specific	Seed layer	1 nm Al + Oxidation					
	Encapsulation	50 nm Al_2O_3 + 100 nm Si_3N_4					
	Channel opening						

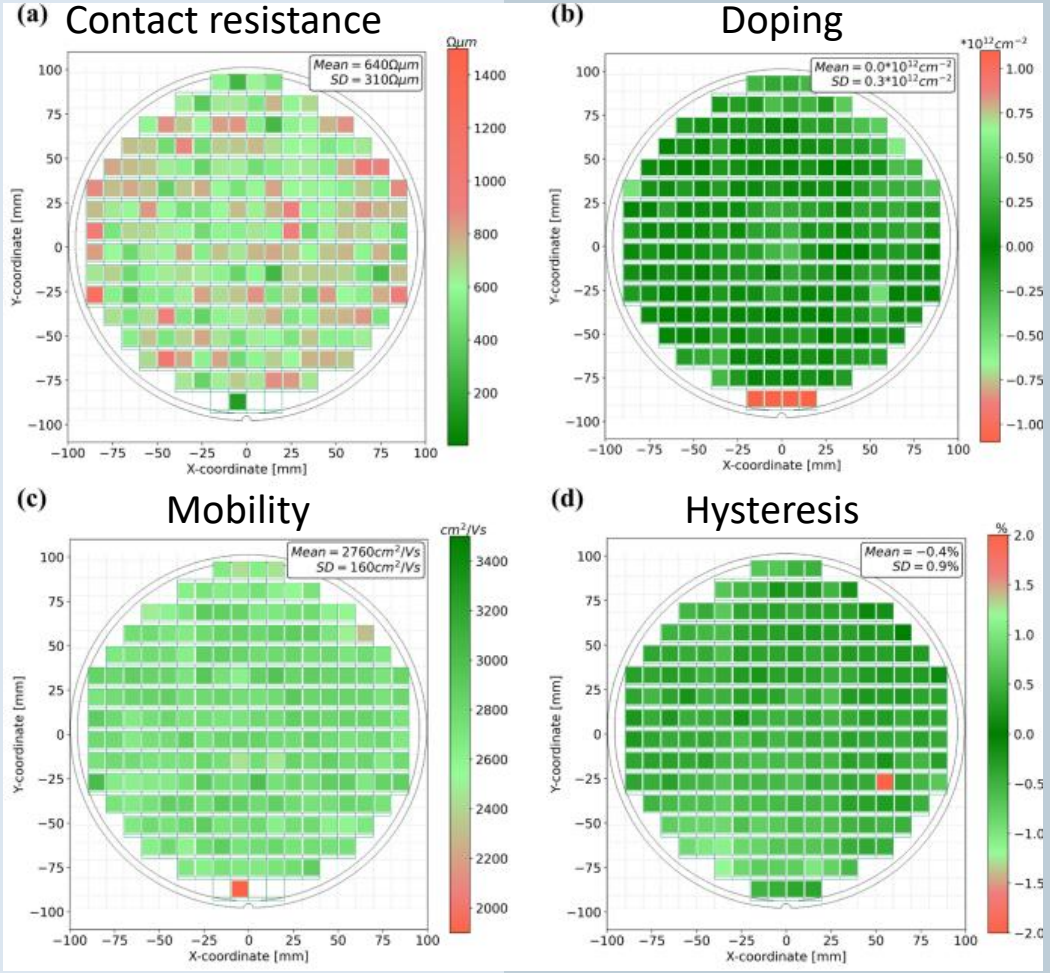


Murros, Anton, et al. "Graphene Field-Effect Transistor Process and Analysis Optimization in 200 mm Pilot-Line Environment." *ACS nano* 20.37 (2026): 25275-25289.

Graphene Process Modules

- 200 mm wafer-scale processing
- Ohmic contacts
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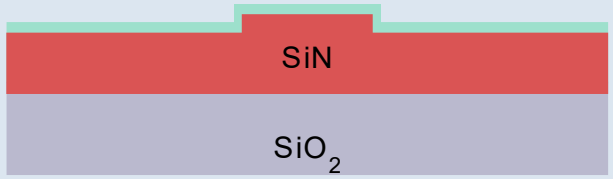




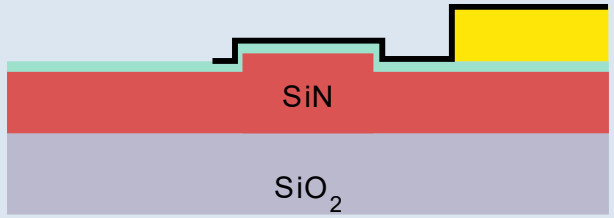
Murros, Anton, et al. "Graphene Field-Effect Transistor Process and Analysis Optimization in 200 mm Pilot-Line Environment." *ACS nano* 20.37 (2026): 25275-25289.

Graphene Modulator Integration

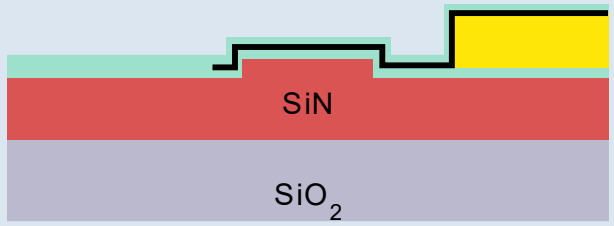
- Passive waveguides
- adhesion layer



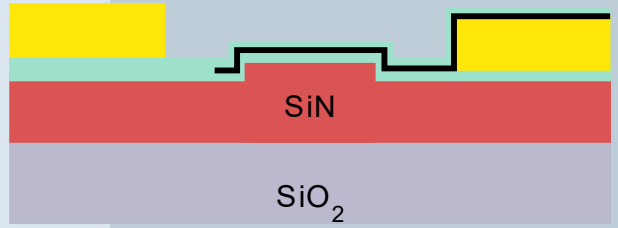
- Bottom contact deposition
- Graphene transfer at Graphenea



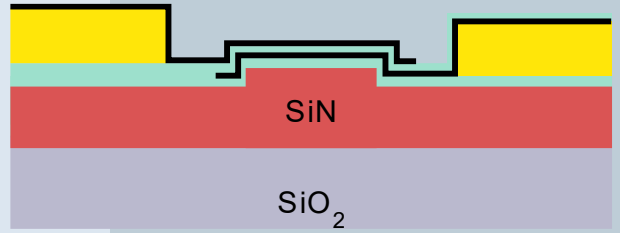
- Dielectric deposition
  - Al seed layer
  - AlO ALD
  - 10-30 nm



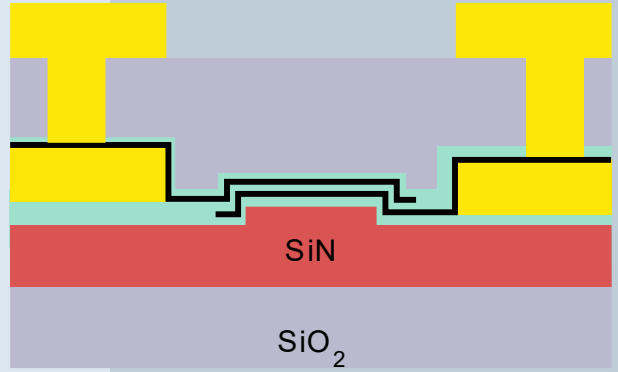
- Bottom contact for 2nd graphene



- Graphene transfer at Graphenea
- Graphene patterning



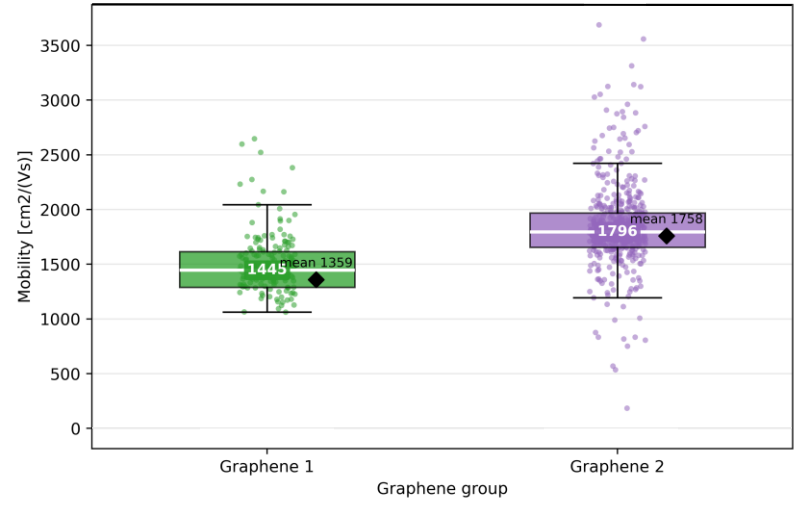
- Protective layer deposition
- Cladding deposition
- Via contacting



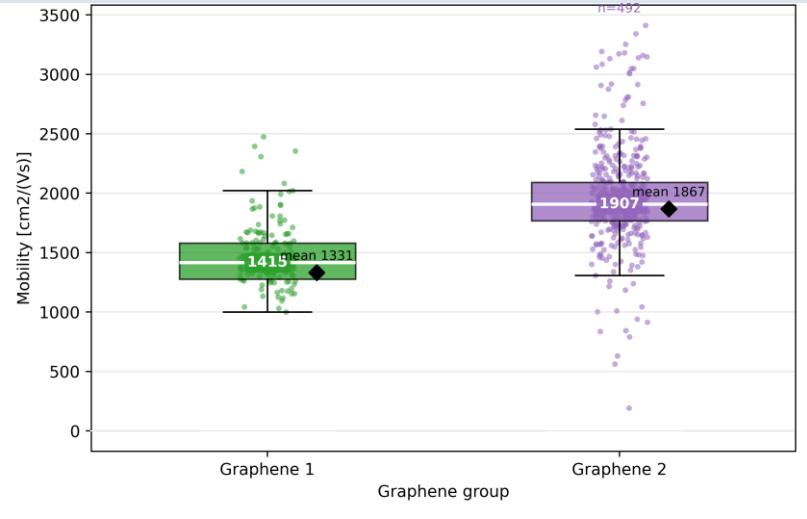
Graphene Quality Control

- Process control monitors confirm similar graphene quality as in CMOS integrated sensor processes
- Decrease in mobility likely due to extra processing steps after graphene transfer

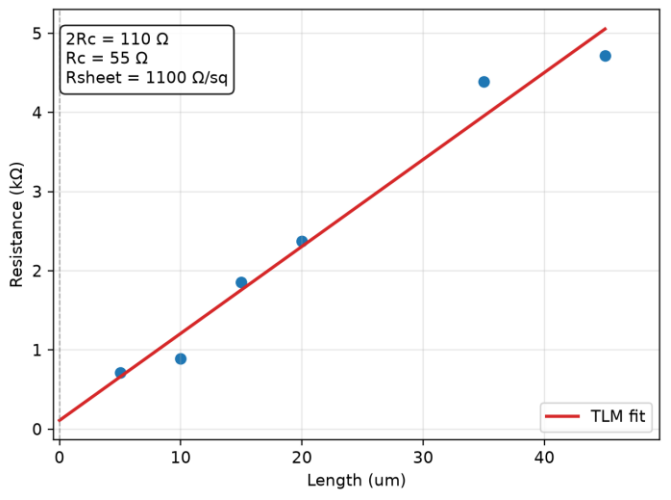
Electron mobility



Hole mobility

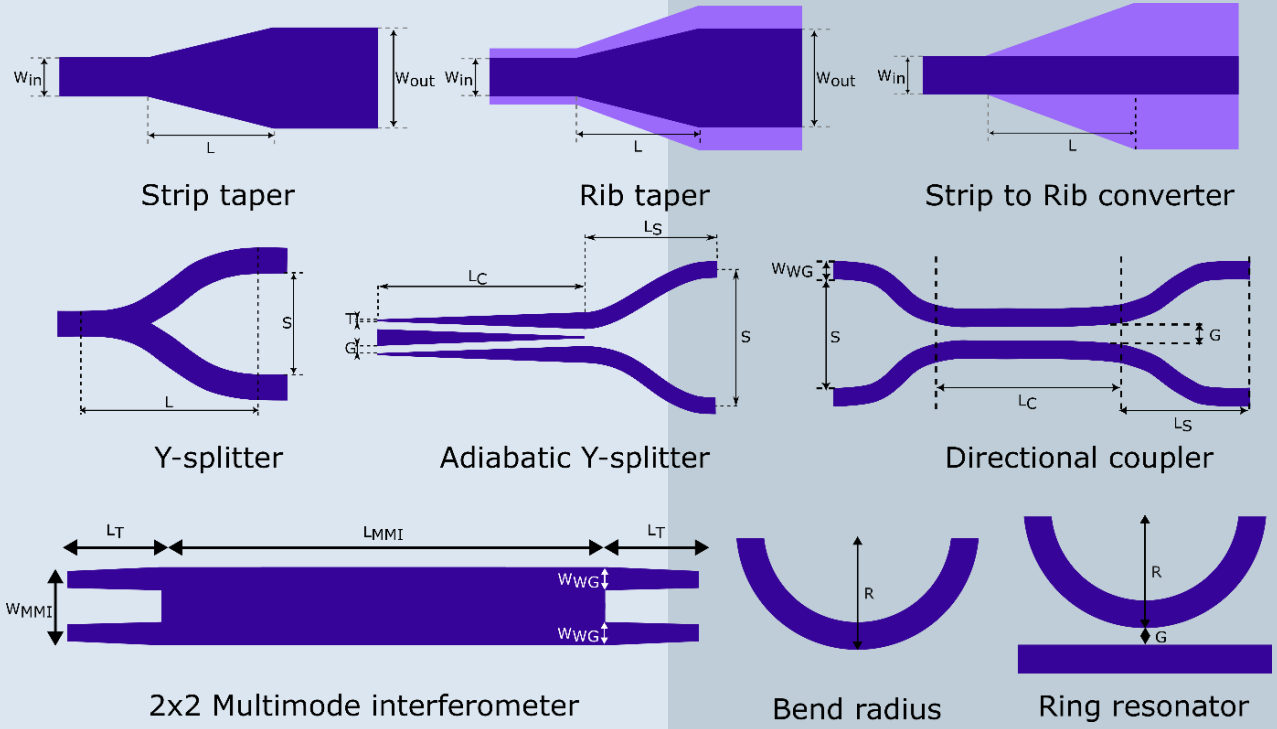


Contact resistance, W = 10µm



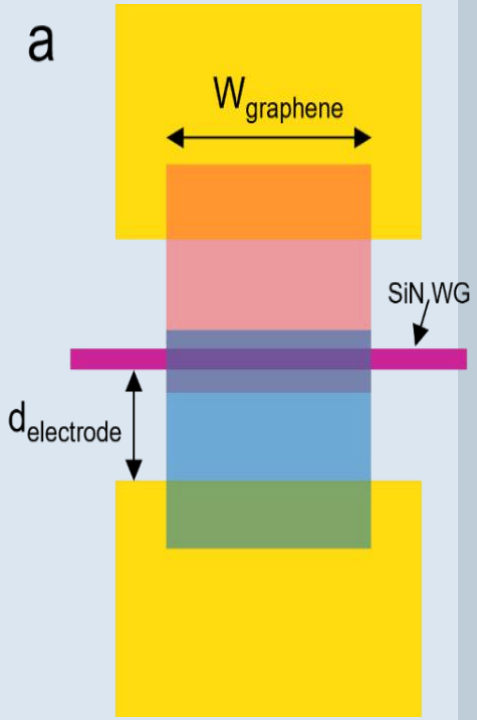
Process Design Kit

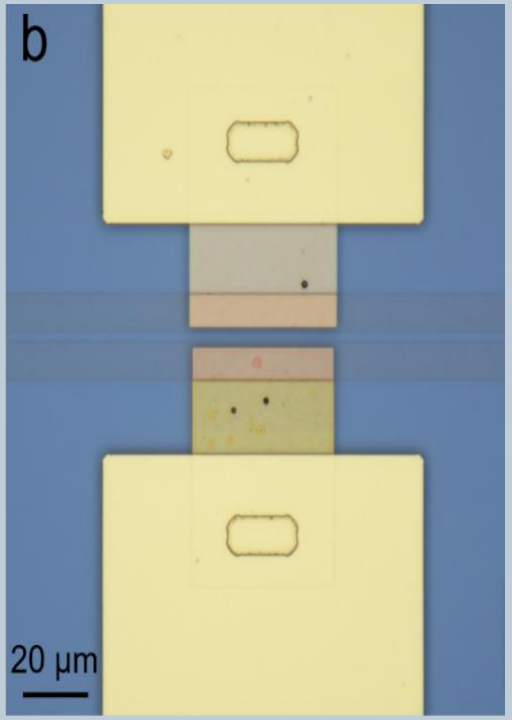
- Built by GDSfactory
- SiN passive platform Includes:
  - Essential waveguide routing building blocks
    - Bends, tapers, couplers
    - Simulated and verified dimensions
  - Wavelengths 900 nm, 1310 nm, and 1550 nm
  - Supports passive circuit simulations
  - DRC
- Graphene modulator
  - First version available only with fixed dimensions



Summary

- **SiN platform:**
  - Verified passive components support 900, 1310 and 1550 nm operation, with propagation losses below 1 dB/cm at 1550 nm.
- **Wafer-scale integration:**
  - Double-layer graphene electro-absorption modulators integrate onto SiN platform at wafer scale
- **Graphene quality:**
  - Graphene quality comparable to VTT's standard process
- **Design readiness:**
  - A GDSfactory-based process design kit supports passive circuit design and simulation





Thanks for listening!

Acknowledgements

VTT
Tarusisko Hirvenoja
Rodolfo Canet Albiach
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Päivi Heimala
Vincent Pelgrin
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Suvi-Tuuli Varjamo (ex-VTT)

Graphenea
Alba Centeno
Amaia Zurutuza
Leire Morillo

2D PILOT LINE

GRAPHENE FLAGSHIP

NEXT 2D IGITS

Funded by
the European Union